Michelly De Souza

List of Publications by Year in descending order

135 papers	1,216 citations	516710 16 h-index	434195 31 g-index
135 all docs	135 docs citations	135 times ranked	585 citing authors

#	Article	IF	Citations
1	Junctionless Multiple-Gate Transistors for Analog Applications. IEEE Transactions on Electron Devices, 2011, 58, 2511-2519.	3.0	234
2	Threshold voltage in junctionless nanowire transistors. Semiconductor Science and Technology, 2011, 26, 105009.	2.0	104
3	Surface-Potential-Based Drain Current Analytical Model for Triple-Gate Junctionless Nanowire Transistors. IEEE Transactions on Electron Devices, 2012, 59, 3510-3518.	3.0	94
4	Cryogenic Operation of Junctionless Nanowire Transistors. IEEE Electron Device Letters, 2011, 32, 1322-1324.	3.9	51
5	Impact of the Series Resistance in the I-V Characteristics of Junctionless Nanowire Transistors and its dependence on the Temperature. Journal of Integrated Circuits and Systems, 2012, 7, 121-129.	0.4	46
6	A physically-based threshold voltage definition, extraction and analytical model for junctionless nanowire transistors. Solid-State Electronics, 2013, 90, 12-17.	1.4	44
7	Charge-based continuous model for long-channel Symmetric Double-Gate Junctionless Transistors. Solid-State Electronics, 2013, 85, 59-63.	1.4	37
8	Substrate Bias Influence on the Operation of Junctionless Nanowire Transistors. IEEE Transactions on Electron Devices, 2014, 61, 1575-1582.	3.0	36
9	An explicit multi-exponential model for semiconductor junctions with series and shunt resistances. Microelectronics Reliability, 2011, 51, 2044-2048.	1.7	29
10	The zero temperature coefficient in junctionless nanowire transistors. Applied Physics Letters, 2012, 101, 062101.	3.3	27
11	Analysis of the leakage current in junctionless nanowire transistors. Applied Physics Letters, 2013, 103, .	3.3	25
12	Analytical Model for the Dynamic Behavior of Triple-Gate Junctionless Nanowire Transistors. IEEE Transactions on Electron Devices, 2016, 63, 856-863.	3.0	24
13	Asymmetric self-cascode configuration to improve the analog performance of SOI nMOS transistors. , 2011, , .		21
14	Compact core model for Symmetric Double-Gate Junctionless Transistors. Solid-State Electronics, 2014, 94, 91-97.	1.4	21
15	On the improvement of DC analog characteristics of FD SOI transistors by using asymmetric self-cascode configuration. Solid-State Electronics, 2016, 117, 152-160.	1.4	18
16	Junctionless nanowire transistors operation at temperatures down to 4.2 K. Semiconductor Science and Technology, 2016, 31, 114001.	2.0	17
17	A New Method for Series Resistance Extraction of Nanometer MOSFETs. IEEE Transactions on Electron Devices, 2017, 64, 2797-2803.	3.0	16
18	Analog Operation Temperature Dependence of nMOS Junctionless Transistors Focusing on Harmonic Distortion. Journal of Integrated Circuits and Systems, 2011, 6, 114-121.	0.4	15

#	ARTICLE	IF	CITATIONS
19	Thin-Film Lateral SOI PIN Diodes for Thermal Sensing Reaching the Cryogenic Regime. Journal of Integrated Circuits and Systems, 2010, 5, 160-167.	0.4	14
20	Effective channel length in Junctionless Nanowire Transistors. , 2015, , .		13
21	Analysis of gate capacitance of n-type junctionless transistors using three-dimensional device simulations. , 2012, , .		11
22	Trap density characterization through low-frequency noise in junctionless transistors. Microelectronic Engineering, 2013, 109, 79-82.	2.4	11
23	Low-frequency noise and effective trap density of short channel p- and n-types junctionless nanowire transistors. Solid-State Electronics, 2014, 96, 22-26.	1.4	11
24	Extraction of the interface trap density energetic distribution in SOI Junctionless Nanowire Transistors. Microelectronic Engineering, 2015, 147, 23-26.	2.4	11
25	A charge-based continuous model for submicron graded-channel nMOSFET for analog circuit simulation. Solid-State Electronics, 2005, 49, 1683-1692.	1.4	10
26	Advantages of graded-channel SOI nMOSFETs for application as source-follower analog buffer. Solid-State Electronics, 2008, 52, 1933-1938.	1.4	10
27	Channel length influence on the analog characteristics of asymmetric self-cascode association of SOI transistors. , 2013, , .		10
28	Analysis of the substrate bias effect on the interface trapped charges in junctionless nanowire transistors through low-frequency noise characterization. Microelectronic Engineering, 2017, 178, 17-20.	2.4	10
29	Temperature and Silicon Film Thickness Influence on the Operation of Lateral SOI PIN Photodiodes for Detection of Short Wavelengths. Journal of Integrated Circuits and Systems, 2011, 6, 107-113.	0.4	10
30	Analog operation of junctionless transistors at cryogenic temperatures. , 2010, , .		9
31	Application of Junctionless Nanowire Transistor in the Self-Cascode Configuration to Improve the Analog Performance. ECS Transactions, 2012, 49, 215-222.	0.5	8
32	Low-Frequency Noise of nMOS and pMOS short channel junctionless nanowire transistors. , 2012, , .		8
33	Study of Matching Properties of Graded-Channel SOI MOSFETs. Journal of Integrated Circuits and Systems, 2008, 3, 69-75.	0.4	8
34	Drain Current and Short Channel Effects Modeling in Junctionless Nanowire Transistors. Journal of Integrated Circuits and Systems, 2013, 8, 116-124.	0.4	8
35	Parameter Extraction in Quadratic Exponential Junction Model with Series Resistance using Global Lateral Fitting. ECS Transactions, 2010, 31, 369-376.	0.5	7
36	Approximate analytical expression for the tersminal voltage in multi-exponential diode models. Solid-State Electronics, 2013, 89, 7-11.	1.4	7

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37	Analysis of Lateral SOI PIN Diodes for the Detection of Blue and UV Wavelengths in a Wide Temperature Range. ECS Transactions, 2010, 31, 199-206.	0.5	6
38	Analog performance of asymmetric self-cascode p-channel fully depleted SOI transistors. , 2012, , .		6
39	Effect of the temperature on on Junctionless Nanowire Transistors electrical parameters down to 4K. , 2014, , .		6
40	Analog performance improvement of self-cascode structures composed by UTBB transistors using back gate bias. , 2015, , .		6
41	Analysis of source-follower buffers implemented with graded-channel SOI nMOSFETs operating at cryogenic temperatures. Cryogenics, 2009, 49, 599-604.	1.7	5
42	Analysis of the Low-Frequency Noise of Junctionless Nanowire Transistors operating in saturation. , 2011, , .		5
43	Asymmetric channel doping profile and temperature reduction influence on the performance of current mirrors implemented with FD SOI nMOSFETs. Microelectronics Reliability, 2013, 53, 848-855.	1.7	5
44	Improved analog operation of junctionless nanowire transistors using back bias. , 2015, , .		5
45	Static and dynamic compact analytical model for junctionless nanowire transistors. Journal of Physics Condensed Matter, 2018, 30, 334002.	1.8	5
46	Junctionless nanowire transistors parameters extraction based on drain current measurements. Solid-State Electronics, 2019, 158, 37-45.	1.4	5
47	Liquid helium temperature analog operation of asymmetric self-cascode FD SOI MOSFETs. , 2012, , .		4
48	Analysis of temperature variation influence on the analog performance of 45° rotated triple-gate nMuGFETs. Solid-State Electronics, 2012, 70, 39-43.	1.4	4
49	Low power highly linear temperature sensor based on SOI lateral PIN diodes. , 2016, , .		4
50	Improved operation of graded-channel SOI nMOSFETs down to liquid helium temperature. Semiconductor Science and Technology, 2016, 31, 114005.	2.0	4
51	Lateral spacers influence on the effective channel length of junctionless nanowire transistors. , 2017, , .		4
52	Accounting for Series Resistance in the Compact Model of Triple-Gate Junctionless Nanowire Transistors. , 2018, , .		4
53	FOSS EKV2.6 Verilog-A Compact MOSFET Model. , 2019, , .		4
54	On the Application of Junctionless Nanowire Transistors in Basic Analog Building Blocks. IEEE Nanotechnology Magazine, 2021, 20, 234-242.	2.0	4

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55	Low temperature influence on the uniaxially strained FD SOI nMOSFETs behavior. Microelectronic Engineering, 2007, 84, 2121-2124.	2.4	3
56	On the Performance of Thin-Film Lateral SOI PIN Diodes as Thermal Sensors in a Wide Temperature Range. ECS Transactions, 2009, 23, 397-404.	0.5	3
57	Drain current model for junctionless nanowire transistors. , 2012, , .		3
58	Low frequency noise in submicron Graded-Channel SOI MOSFETs. , 2013, , .		3
59	Analysis of harmonic distortion of asymmetric self-cascode association of SOI nMOSFETs operating in saturation. , 2014, , .		3
60	Technological parameters scaling influence on the analog performance of Graded-Channel SOI nMOSFET transistors. , 2014, , .		3
61	Use of back gate bias to enhance the analog performance of planar FD and UTBB SOI transistors-based self-cascode structures. , 2015, , .		3
62	A new series resistance extraction method for junctionless nanowire transistors. , 2016, , .		3
63	Use of back gate bias to improve the performance of n- and p-type UTBB transistors-based self-cascode structures applied to current mirrors. , 2016, , .		3
64	Junctionless Nanowire Transistors Based Wilson Current Mirror Configuration. , 2021, , .		3
65	Physical Insights on the Dynamic Response of SOI n- and p-Type Junc-tionless Nanowire Transistors. Journal of Integrated Circuits and Systems, 2018, 13, 1-7.	0.4	3
66	Experimental Assessment of Variability in Junctionless Nanowire nMOS Transistors. , 2021, , .		3
67	Graded-Channel SOI nMOSFET Model Valid for Harmonic Distortion Evaluation. , 0, , .		2
68	Comparison between the behavior of submicron graded-channel SOI nMOSFETs with fully- and partially-depleted operations in a wide temperature range. , 2010, , .		2
69	Characterization of Thin-Film SOI PIN Diodes from Cryogenic to Above Room Temperatures Using an Explicit I-V Multi-Branch Model. ECS Transactions, 2011, 39, 171-178.	0.5	2
70	Impact of Substrate Rotation and Temperature on the Mobility and Series Resistance of Triple-Gate SOI nMOSFETs. ECS Transactions, 2011, 39, 223-230.	0.5	2
71	Accounting for Short Channel Effects in the Drain Current Modeling of Junctionless Nanowire Transistors. ECS Transactions, 2012, 49, 207-214.	0.5	2
72	The role of the incomplete ionization on the operation of Junctionless Nanowire Transistors. , 2012, , .		2

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73	Harmonic distortion analysis of short channel junctionless nanowire transistors operating as amplifiers. , 2013, , .		2
74	Analysis of charges densities in multiple-gates SOI nMOS junctionless. , 2013, , .		2
75	Effective mobility analysis of n- and p-types SOI junctionless nanowire transistors. , 2014, , .		2
76	Advantages of subthreshold operation of asymmetric self-cascode SOI transistors aiming at analog circuit applications. , 2015, , .		2
77	Experimental and simulation analysis of electrical characteristics of commonâ€source current mirrors implemented with asymmetric selfâ€cascode siliconâ€onâ€insulator nâ€channel metalâ€"oxideâ€"semiconductor fieldâ€effect transistors. IET Circuits, Devices and Systems, 2016, 10, 349-355.	1.4	2
78	Influence of the crystal orientation on the operation of junctionless nanowire transistors. , 2016, , .		2
79	Modeling the Interface Trap Density Influence on Junctionless Nanowire Transistors Behavior. , 2018, , .		2
80	Effect of the back bias on the analog performance of standard FD and UTBB transistors-based self-cascode structures. Semiconductor Science and Technology, 2017, 32, 095005.	2.0	2
81	Junctionless Nanowire Transistors Based Common-Source Current Mirror. , 2021, , .		2
82	Channel Length Influence on the Performance of Source-Follower Buffers Implemented with Graded-Channel SOI nMOSFETs. ECS Transactions, 2008, 14, 263-272.	0.5	1
83	Performance of Common-Source, Cascode and Wilson Current Mirrors Implemented with Graded-Channel SOI nMOSFETs in a Wide Temperature Range. ECS Transactions, 2009, 19, 265-270.	0.5	1
84	Analysis of the Low-Frequency Noise in Graded-Channel and Standard SOI nMOSFET. ECS Transactions, 2010, 31, 359-366.	0.5	1
85	Electrical characterization of SOI solar cells in a wide temperature range. , 2010, , .		1
86	Performance of Ultra-Low-Power SOI CMOS Diodes Operating at Low Temperatures. ECS Transactions, 2011, 35, 325-330.	0.5	1
87	Comparison between SOI nMOSFET's under Uniaxial and Biaxial Mechanical Stress in Analog Applications. ECS Transactions, 2011, 39, 37-44.	0.5	1
88	Intrinsic Gate Capacitances of n-type Junctionless Nanowire Transistors Using a Three-Dimensional Device Simulation and Experimental Measurements. ECS Transactions, 2012, 49, 231-239.	0.5	1
89	Non-linear behavior of Junctionless nanowire transistors operating in the linear regime. , 2013, , .		1
90	Analytical model for potential in double-gate juntionless transistors. , 2013, , .		1

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91	Performance of Junctionless Nanowire MOSFET as a Quasi-Linear Resistor. ECS Transactions, 2013, 53, 115-120.	0.5	1
92	Analog Behavior of Submicron Graded-Channel SOI MOSFETs Varying Channel Length, Doping Concentration and Temperature. ECS Transactions, 2013, 53, 149-154.	0.5	1
93	Analog performance of short-channel asymmetric self-cascode of junctionless nanowire nMOS transistors. , 2014, , .		1
94	Asymmetric self-cascode FD SOI nMOSFETS harmonic distortion at cryogenic temperatures. , 2014, , .		1
95	Quasi-static analytical model for the dynamic operation of triple-gate junctionless nanowire transistors. , 2015, , .		1
96	On the origin of low-frequency noise of submicron Graded-Channel fully depleted SOI nMOSFETs. , 2015, , .		1
97	Ultra-low-power diodes using junctionless nanowire transistors. , 2015, , .		1
98	Asymmetric Self-Cascode versus Graded-Channel SOI nMOSFETs for analog applications. , 2015, , .		1
99	Physical insights on the dynamic response of junctionless nanowire transistors. , 2016, , .		1
100	Errata to â€œSurface-Potential-Based Drain Current Analytical Model for Triple-Gate Junctionless Nanowire Transistorsâ€•[Dec 12 3510-3518]. IEEE Transactions on Electron Devices, 2016, 63, 527-527.	3.0	1
101	Improved analog performance of SOI Nanowire nMOSFETs Self-Cascode through back-biasing. , 2017, , .		1
102	Channel width influence on the analog performance of the asymmetric self-cascode FD SOI nMOSFETs. , 2017, , .		1
103	Experimental evaluation of mismatching on the analog characteristics of GC SOI MOSFETs. , 2017, , .		1
104	Influence of the Intrinsic Length on the Behavior of PIN Diodes Fabricated on SOI Substrates Working as Solar Cells. , 2018, , .		1
105	Design benefits of self-cascode configuration for analog applications in 28 FDSOI. , 2018, , .		1
106	Modeling of Thin-Film Lateral SOI PIN Diodes with an Alternative Multi-Branch Explicit Current Model. Journal of Integrated Circuits and Systems, 2012, 7, 92-99.	0.4	1
107	Subthreshold Operation of Self-Cascode Structure Using UTBB FD SOI Planar MOSFETs. , 2019, , .		1
108	Analysis of Capacitances in Asymmetric Self-Cascode SOI nMOSFETs. , 2021, , .		1

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109	Analysis of Mobility in Graded-Channel SOI Transistors Aiming at Circuit Simulation. Journal of Integrated Circuits and Systems, 2020, 15, 1-5.	0.4	1
110	Variability Modeling in Triple-Gate Junctionless Nanowire Transistors. IEEE Transactions on Electron Devices, 2022, 69, 4730-4736.	3.0	1
111	Monte Carlo simulation of graded-channel fully depleted SOI nMOSFETs. , 2011, , .		0
112	Liquid Helium Temperature Operation of Graded-Channel SOI nMOSFETs. ECS Transactions, 2012, 49, 135-144.	0.5	0
113	Comparative Study of Biaxial and Uniaxial Mechanical Stress Influence on the Low Frequency Noise of Fully Depleted SOI nMOSFETs Operating in Triode and Saturation Regime. ECS Transactions, 2012, 49, 77-83.	0.5	0
114	The influence of the substrate bias in Junctionless nanowire transistors. , 2013, , .		0
115	Effect of high temperature on analog parameters of Asymmetric Self-Cascode SOI nMOSFETs. , 2014, , .		0
116	Analog operation of Junctionless Nanowire Transistors down to liquid helium temperature. , 2014, , .		0
117	Effect of channel doping concentration on the harmonic distortion of asymmetric n- and p-type self-cascode MOSFETs. , 2015, , .		0
118	Low-frequency noise in asymmetric self-cascode FD SOI nMOSFETs. , 2016, , .		0
119	Low-frequency noise of submicron graded-channel SOI nMOSFETs at high temperature. , 2016, , .		0
120	A new method for junctionless transistors parameters extraction. , 2017, , .		0
121	Analysis of p-type Junctionless nanowire transistors with different crystallographic orientations. , 2017, , .		0
122	Analog performance of self-cascode SOI nanowires nMOSFETs aiming at low-power applications. , 2017, , .		0
123	Experimental comparative analysis between junctionless and inversion mode nanowire transistors down to 10 nm-long channel lengths. , 2017, , .		0
124	Back bias influence on low-frequency noise of n-type nanowires SOI MOSFETs. , 2018, , .		0
125	Asymmetric Self-Cascode Current-Voltage Constructing Algorithm for Analog Figures-of-Merit Extraction. , 2018, , .		0
126	Numerical Simulation and Analysis of Transistor Channel Length and Doping Mismatching in GC SOI nMOSFETs Analog Figures of Merit. , 2018, , .		0

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127	Linearity Enhancement in Asymmetric Self-Cascode Composed by FD SOI nMOSFETs. , 2018, , .		0
128	Harmonic Distortion in Symmetric and Asymmetric Self-Cascodes of UTBB FD SOI Planar MOSFETs. , 2019, , .		0
129	Analysis of the Thermal Properties of Self-Cascode Structures Composed by UTBB Transistors. , 2020, , .		0
130	Strategy for Simulation of Analog Circuits with GCSOI MOSFET using BSIM SOI model. , 2021, , .		0
131	Influence of Geometrical Parameters on the DC Analog Behavior of the Asymmetric Self-Cascode FD SOI nMOSFETs. Journal of Integrated Circuits and Systems, 2018, 13, 1-7.	0.4	0
132	Analysis of Mismatching on the Analog Characteristics of GC SOI MOSFETs. Journal of Integrated Circuits and Systems, 2018, 13, 1-8.	0.4	0
133	Temperature, Silicon Thickness and Intrinsic Length Influence on the Operation of Lateral SOI PIN Photodiodes. Journal of Integrated Circuits and Systems, 2020, 15, 1-5.	0.4	0
134	Analysis of Current Mirrors with Asymmetric Self-Cascode Association of SOI MOSFETs through SPICE Simulations. Journal of Integrated Circuits and Systems, 2020, 15, 1-5.	0.4	0
135	Experimental Demonstration of Î©-Gate SOI Nanowire MOS Transistorsâ€™ Mobility Variation Induced by Substrate Bias. IEEE Transactions on Electron Devices, 2022, 69, 4022-4028.	3.0	0