Tuo-Hung Hou

List of Publications by Year in Descending Order

135 papers	3,781 citations	31 h-index	59 g-index
164 ext. papers	5,125 ext. citations	4.3 avg, IF	5.42 L-index

#	Paper	IF	Citations
135	Device quantization policy in variation-aware in-memory computing design.. *Scientific Reports*, **2022**, 12, 112	4.9	2
134	Resistive Random Access Memory (RRAM) Technology: From Material, Device, Selector, 3D Integration to Bottom-Up Fabrication. *Kluwer International Series in Electronic Materials: Science and Technology*, **2022**, 33-64		
133	Voltage-Time Transformation Model for Threshold Switching Spiking Neuron Based on Nucleation Theory.. *Frontiers in Neuroscience*, **2022**, 16, 868671	5.1	
132	Hardware-Robust In-RRAM-Computing for Object Detection. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2022**, 1-1	5.2	
131	Two-Dimensional Materials-Based Static Random-Access Memory.. *Advanced Materials*, **2021**, e2107894	24	0
130	Standards for the Characterization of Endurance in Resistive Switching Devices. *ACS Nano*, **2021**,	16.7	36
129	. *IEEE Transactions on Electron Devices*, **2021**, 68, 6082-6086	2.9	
128	BiOSe-Based Memristor-Aided Logic. *ACS Applied Materials & Interfaces*, **2021**, 13, 15391-15398	9.5	7
127	Progress and Benchmark of Spiking Neuron Devices and Circuits. *Advanced Intelligent Systems*, **2021**, 3, 2100007	6	10
126	. *IEEE Electron Device Letters*, **2021**, 42, 1464-1467	4.4	6
125	Dimensionally anisotropic graphene with high mobility and a high on□off ratio in a three-terminal RRAM device. *Materials Chemistry Frontiers*, **2020**, 4, 1756-1763	7.8	4
124	Semi-Empirical RC Circuit Model for Non-Filamentary Bi-Layer OxRAM Devices. *IEEE Transactions on Electron Devices*, **2020**, 67, 1348-1352	2.9	1
123	Exploiting analogue OxRAM conductance modulation for contrast enhancement application. *Electronics Letters*, **2020**, 56, 594-597	1.1	
122	Nonvolatile molecular memory with the multilevel states based on MoS nanochannel field effect transistor through tuning gate voltage to control molecular configurations. *Nanotechnology*, **2020**, 31, 275204	3.4	2
121	SLIM: Simultaneous Logic-in-Memory Computing Exploiting Bilayer Analog OxRAM Devices. *Scientific Reports*, **2020**, 10, 2567	4.9	242
120	Strong Read and Write Interference Induced by Breakdown Failure in Crossbar Arrays. *IEEE Transactions on Electron Devices*, **2020**, 67, 5497-5504	2.9	3
119	Pulse-Mediated Electronic Tuning of the MoS2□Perovskite Ferroelectric Field Effect Transistors. *ACS Applied Electronic Materials*, **2020**, 2, 3843-3852	4	1

118	Promising Engineering Approaches for Improving the Reliability of HfZrOx 2-D and 3-D Ferroelectric Random Access Memories. *IEEE Transactions on Electron Devices*, **2020**, 67, 5479-5483	2.9	3
117	Ferroelectric HfZrO2 With Electrode Engineering and Stimulation Schemes as Symmetric Analog Synaptic Weight Element for Deep Neural Network Training. *IEEE Transactions on Electron Devices*, **2020**, 67, 4201-4207	2.9	13
116	Stochastic STT-MRAM Spiking Neuron Circuit **2020**,		2
115	Drain-Bias Transient Instability of Amorphous Indium Gallium Zinc Oxide Thin-Film Transistors. *IEEE Transactions on Electron Devices*, **2020**, 67, 4526-4529	2.9	
114	Polymorphism Control of Layered MoTe through Two-Dimensional Solid-Phase Crystallization. *Scientific Reports*, **2019**, 9, 8810	4.9	8
113	NV-BNN **2019**,		9
112	Local Modulation of Electrical Transport in 2D Layered Materials Induced by Electron Beam Irradiation. *ACS Applied Electronic Materials*, **2019**, 1, 684-691	4	12
111	A Fluorographene-Based Synaptic Transistor. *Advanced Materials Technologies*, **2019**, 4, 1900422	6.8	18
110	Extremely Compact Integrate-and-Fire STT-MRAM Neuron: A Pathway toward All-Spin Artificial Deep Neural Network **2019**,		10
109	A Comprehensive Modeling Framework for Ferroelectric Tunnel Junctions **2019**,		13
108	Sub-nA Low-Current HZO Ferroelectric Tunnel Junction for High-Performance and Accurate Deep Learning Acceleration **2019**,		14
107	Effective N-methyl-2-pyrrolidone wet cleaning for fabricating high-performance monolayer MoS2 transistors. *Nano Research*, **2019**, 12, 303-308	10	6
106	Recommended Methods to Study Resistive Switching Devices. *Advanced Electronic Materials*, **2019**, 5, 1800143	6.4	297
105	Mitigating Asymmetric Nonlinear Weight Update Effects in Hardware Neural Network Based on Analog Resistive Synapse. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2018**, 8, 116-124	5.2	57
104	High-Performance Double-Gate $alpha $ -InGaZnO ISFET pH Sensor Using a HfO2 Gate Dielectric. *IEEE Transactions on Electron Devices*, **2018**, 65, 237-242	2.9	28
103	Optimizing Incremental Step Pulse Programming for RRAM Through Device Circuit Co-Design. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 617-621	3.5	6
102	Programmable Synaptic Metaplasticity and below Femtojoule Spiking Energy Realized in Graphene-Based Neuromorphic Memristor. *ACS Applied Materials & Interfaces*, **2018**, 10, 20237-20243	8.5	48
101	Interchangeable Hebbian and Anti-Hebbian STDP Applied to Supervised Learning in Spiking Neural Network **2018**,		3

100	Large-Area 2D Layered MoTe2 by Physical Vapor Deposition and Solid-Phase Crystallization in a Tellurium-Free Atmosphere. *Advanced Materials Interfaces*, **2017**, 4, 1700157	4.6	41
99	Statistical study of RRAM MLC SET variability induced by filament morphology **2017**,		1
98	Internal current amplification induced by dielectric hole trapping in monolayer MoS transistor. *Nanotechnology*, **2017**, 28, 475204	3.4	
97	AC stress and electronic effects on SET switching of HfO2 RRAM. *Applied Physics Letters*, **2017**, 111, 093502	3.4	1
96	Resistive random access memory (RRAM) technology: From material, device, selector, 3D integration to bottom-up fabrication. *Journal of Electroceramics*, **2017**, 39, 21-38	1.5	57
95	Challenges and opportunities toward online training acceleration using RRAM-based hardware neural network **2017**,		19
94	TaOx-/TiO2-Based Synaptic Devices **2017**, 73-95		3
93	32-nm Multigate Si-nTFET With Microwave-Annealed Abrupt Junction. *IEEE Transactions on Electron Devices*, **2016**, 63, 1808-1813	2.9	8
92	High-Voltage Amorphous InGaZnO TFT With Al2O3 High- k Dielectric for Low-Temperature Monolithic 3-D Integration. *IEEE Transactions on Electron Devices*, **2016**, 63, 3944-3949	2.9	25
91	Large-area few-layer MoS2deposited by sputtering. *Materials Research Express*, **2016**, 3, 065007	1.7	28
90	1-V Full-Swing Depletion-Load a-InGaZnO Inverters for Back-End-of-Line Compatible 3D Integration. *IEEE Electron Device Letters*, **2016**, 37, 441-444	4.4	18
89	Interface engineered HfO2-based 3D vertical ReRAM. *Journal Physics D: Applied Physics*, **2016**, 49, 215102	3	19
88	Grain size and plasma doping effects on CVD-based 2D transition metal dichalcogenide **2016**,		2
87	Abnormal positive bias stress instability of InGaZnO thin-film transistors with low-temperature Al2O3 gate dielectric. *Applied Physics Letters*, **2016**, 108, 033502	3.4	45
86	Low-Voltage InGaZnO Ion-Sensitive Thin-Film Transistors Fabricated by Low-Temperature Process. *IEEE Transactions on Electron Devices*, **2016**, 63, 5060-5063	2.9	12
85	3D Ta/TaO x /TiO2/Ti synaptic array and linearity tuning of weight update for hardware neural network applications. *Nanotechnology*, **2016**, 27, 365204	3.4	101
84	3D resistive RAM cell design for high-density storage class memory—a review. *Science China Information Sciences*, **2016**, 59, 1	3.4	39
83	Suspended Diamond-Shaped Nanowire With Four {111} Facets for High-Performance Ge Gate-All-Around FETs. *IEEE Transactions on Electron Devices*, **2016**, 63, 3837-3843	2.9	2

82	Crossbar array of selector-less TaOx/TiO2 bilayer RRAM. *Microelectronics Reliability*, **2015**, 55, 2220-2223	1.2	23
81	Categorization of Multilevel-Cell Storage-Class Memory: An RRAM Example. *IEEE Transactions on Electron Devices*, **2015**, 62, 2510-2516	2.9	11
80	Grain size effect of monolayer MoS2 transistors characterized by second harmonic generation mapping **2015**,		1
79	A Study of Blocking and Tunnel Oxide Engineering on Double-Trapping (DT) BE-SONOS Performance **2015**,		1
78	Optically initialized robust valley-polarized holes in monolayer WSe2. *Nature Communications*, **2015** , 6, 8963	17.4	120
77	**2015**,		110
76	Diamond-shaped Ge and Ge0.9Si0.1 gate-all-around nanowire FETs with four {111} facets by dry etch technology **2015**,		12
75	Characterization and Modeling of Nonfilamentary Ta/TaOx/TiO2/Ti Analog Synaptic Device. *Scientific Reports*, **2015**, 5, 10150	4.9	122
74	Neuromorphic pattern learning using HBM electronic synapse with excitatory and inhibitory plasticity **2015**,		5
73	Fully parallel write/read in resistive synaptic array for accelerating on-chip learning. *Nanotechnology*, **2015**, 26, 455204	3.4	78
72	Multi-level control of conductive nano-filament evolution in HfO2 ReRAM by pulse-train operations. *Nanoscale*, **2014**, 6, 5698-702	7.7	113
71	Homogeneous barrier modulation of TaOx/TiO2 bilayers for ultra-high endurance three-dimensional storage-class memory. *Nanotechnology*, **2014**, 25, 165202	3.4	59
70	Improved multi-level control of RRAM using pulse-train programming **2014**,		4
69	**2014**,		63
68	3D vertical TaOx/TiO2 RRAM with over 103 self-rectifying ratio and sub-μA operating current **2013**,		9
67	Flexible Three-Bit-Per-Cell Resistive Switching Memory Using a-IGZO TFTs. *IEEE Electron Device Letters*, **2013**, 34, 1265-1267	4.4	17
66	Statistical Model and Rapid Prediction of RRAM SET Speed–Disturb Dilemma. *IEEE Transactions on Electron Devices*, **2013**, 60, 3760-3766	2.9	34
65	On the potential of CRS, 1D1R, and 1S1R crossbar RRAM for storage-class memory **2013**,		3

64	Dependence of Read Margin on Pull-Up Schemes in High-Density One Selector One Resistor Crossbar Array. *IEEE Transactions on Electron Devices*, **2013**, 60, 420-426	2.9	78
63	. *IEEE Electron Device Letters*, **2013**, 34, 885-887	4.4	34
62	Reversible transition of resistive switching induced by oxygen-vacancy and metal filaments in HfO2. *Solid-State Electronics*, **2013**, 89, 167-170	1.7	20
61	Switching Mode and Mechanism in Binary Oxide Resistive Random Access Memory Using Ni Electrode. *Japanese Journal of Applied Physics*, **2013**, 52, 031801	1.4	16
60	Design and optimization methodology for 3D RRAM arrays **2013**,		30
59	Rapid Prediction of RRAM RESET-State Disturb by Ramped Voltage Stress. *IEEE Electron Device Letters*, **2012**, 33, 597-599	4.4	16
58	Redox Molecules for a Resonant Tunneling Barrier in Nonvolatile Memory. *IEEE Transactions on Electron Devices*, **2012**, 59, 1189-1198	2.9	6
57	Polycrystalline silicon thin-film transistor with nickel titanium oxide by sol gel spin-coating and nitrogen implantation. *Solid-State Electronics*, **2012**, 78, 11-16	1.7	
56	Amorphous InGaZnO Thin-Film Transistors Compatible With Roll-to-Roll Fabrication at Room Temperature. *IEEE Electron Device Letters*, **2012**, 33, 47-49	4.4	43
55	RRAM SET speed-disturb dilemma and rapid statistical prediction methodology **2012**,		11
54	Multi-bit-per-Cell a-IGZO TFT resistive-switching memory for system-on-plastic applications **2012**,		3
53	Flexible One Diode One Resistor Crossbar Resistive-Switching Memory. *Japanese Journal of Applied Physics*, **2012**, 51, 04DD09	1.4	14
52	Flexible One Diode One Resistor Crossbar Resistive-Switching Memory. *Japanese Journal of Applied Physics*, **2012**, 51, 04DD09	1.4	18
51	Fabrication and Characterization of High-k Dielectric Nickel Titanate Thin Films Using a Modified Sol Gel Method. *Journal of the American Ceramic Society*, **2011**, 94, 250-254	3.8	29
50	Stackable nonvolatile memory with ultra thin polysilicon film and low-leakage (Ti,Dy)xOy for low processing temperature and low operating voltages. *Microelectronic Engineering*, **2011**, 88, 3462-3465	2.5	
49	Integration of Self-Assembled Redox Molecules in Flash Memory Devices. *IEEE Transactions on Electron Devices*, **2011**, 58, 826-834	2.9	28
48	Electrode dependence of filament formation in HfO2 resistive-switching memory. *Journal of Applied Physics*, **2011**, 109, 084104	2.5	227
47	One selector-one resistor (1S1R) crossbar array for high-density flexible memory applications **2011**,		70

46	Bipolar Nonlinear $hbox{Ni/TiO}_{2}hbox{/}hbox{Ni}$ Selector for 1S1R Crossbar Array Applications. *IEEE Electron Device Letters*, **2011**, 32, 1427-1429	4.4	140
45	Novel Two-Bit-per-Cell Resistive-Switching Memory for Low-Cost Embedded Applications. *IEEE Electron Device Letters*, **2011**, 32, 1662-1664	4.4	3
44	Low-IRESET unipolar HfO2 RRAM and tunable resistive-switching mode via interface engineering **2011**,		1
43	Evolution of RESET current and filament morphology in low-power HfO2 unipolar resistive switching memory. *Applied Physics Letters*, **2011**, 98, 103511	3.4	39
42	Strained Silicon Technology: Mobility Enhancement and Improved Short Channel Effect Performance by Stress Memorization Technique on nFET Devices. *Journal of the Electrochemical Society*, **2010**, 157, H497	3.9	2
41	Transition of stable rectification to resistive-switching in Ti/TiO2/Pt oxide diode. *Applied Physics Letters*, **2010**, 96, 262901	3.4	139
40	Characterization of Highly Strained nFET Device Performance and Channel Mobility with SMT. *Journal of the Electrochemical Society*, **2010**, 157, H705	3.9	
39	Low power nonvolatile SRAM circuit with integrated low voltage nanocrystal PMOS Flash **2010**,		2
38	Stability of La2O3MetalInsulatorMetal Capacitors under Constant Voltage Stress. *Japanese Journal of Applied Physics*, **2010**, 49, 04DB16	1.4	7
37	Statistical Metrology of Metal Nanocrystal Memories With 3-D Finite-Element Analysis. *IEEE Transactions on Electron Devices*, **2009**, 56, 1729-1735	2.9	8
36	Material and electrical characterization of stackable planar polysilicon TFT flash memory cell with metal nanocrystals and high-k dielectrics **2008**,		1
35	Flash Memory Scaling: From Material Selection to Performance Improvement. *Materials Research Society Symposia Proceedings*, **2008**, 1071, 1		2
34	Nonvolatile memory with molecule-engineered tunneling barriers. *Applied Physics Letters*, **2008**, 92, 153109	3.4	8
33	Modeling of Multi-layer Nanocrystal Memory. *Device Research Conference, IEEE Annual*, **2007**,		1
32	Fermi-Level Pinning in Nanocrystal Memories. *IEEE Electron Device Letters*, **2007**, 28, 103-106	4.4	21
31	Enhanced Electrostatics for Low-Voltage Operations in Nanocrystal Based Nanotube/Nanowire Memories. *IEEE Nanotechnology Magazine*, **2007**, 6, 22-28	2.6	8
30	Design Optimization of Metal Nanocrystal MemoryPart I: Nanocrystal Array Engineering. *IEEE Transactions on Electron Devices*, **2006**, 53, 3095-3102	2.9	67
29	Design Optimization of Metal Nanocrystal MemoryPart II: Gate-Stack Engineering. *IEEE Transactions on Electron Devices*, **2006**, 53, 3103-3109	2.9	28

28	Effects of Metal Nanocrystals and Traps in Tunneling Rate Measurements in Metal Nanocrystal Based Carbon Nanotube Memory. *Materials Research Society Symposia Proceedings*, **2006**, 963, 1		
27	Process Integration of Composite High-k Tunneling Dielectric for Nanocrystal Based Carbon Nanotube Memory. *Materials Research Society Symposia Proceedings*, **2006**, 961, 1		
26	Three-dimensional analytical modeling of nanocrystal memory electrostatics. *Journal of Applied Physics*, **2006**, 99, 114516	2.5	2
25	Programable molecular orbital states of C60 from integrated circuits. *Applied Physics Letters*, **2006**, 89, 253113	3.4	16
24	Metal nanocrystal/nitride heterogeneous-stack floating gate memory **2005**,		3
23	Asymmetric electric field enhancement in nanocrystal memories. *IEEE Electron Device Letters*, **2005**, 26, 879-881	4.4	24
22	Reliability studies of Hf-doped and NH3-nitrided gate dielectric for advanced CMOS application. *IET Circuits, Devices and Systems*, **2005**, 152, 407		
21	Nonvolatile memory with a metal nanocrystal/nitride heterogeneous floating-gate. *IEEE Transactions on Electron Devices*, **2005**, 52, 2697-2702	2.9	39
20	Subnanometer Scaling of HfO[sub 2]/Metal Electrode Gate Stacks. *Electrochemical and Solid-State Letters*, **2004**, 7, G164		23
19	Characterization of high-k gate dielectric and metal gate electrode semiconductor samples with a total reflection X-ray fluorescence spectrometer. *Spectrochimica Acta, Part B: Atomic Spectroscopy*, **2004**, 59, 1227-1234	3.1	11
18	Effective improvement of high-k Hf-silicate□silicon interface with thermal nitridation. *Electronics Letters*, **2003**, 39, 421	1.1	5
17	HfO2□HfSixOy high-K gate stack with very low leakage current for low-power poly-Si gated CMOS application. *Electronics Letters*, **2003**, 39, 692	1.1	1
16	High-k gate stacks for planar, scaled CMOS integrated circuits. *Microelectronic Engineering*, **2003**, 69, 152-167	2.5	49
15	SIMS depth profiling of advanced gate dielectric materials. *Applied Surface Science*, **2003**, 203-204, 409-413	0.7	20
14	Effect of polycrystalline-silicon gate types on the opposite flatband voltage shift in n-type and p-type metal□oxide□semiconductor field-effect transistors for high-k-HfO2 dielectric. *Applied Physics Letters*, **2003**, 83, 308-310	3.4	28
13	Origin of the threshold voltage instability in SiO2/HfO2 dual layer gate dielectrics. *IEEE Electron Device Letters*, **2003**, 24, 87-89	4.4	280
12	Improved current drivability and poly-gate depletion of submicron PMOSFET with poly-SiGe gate and ultra-thin nitride gate dielectric. *Solid-State Electronics*, **2002**, 46, 597-599	1.7	2
11	Dramatic reduction of gate leakage current in 1.61 nm HfO2 high-k dielectric poly-silicon gate with Al2O3 capping layer. *Electronics Letters*, **2002**, 38, 1223	1.1	5

10	To optimize electrical properties of the ultrathin (1.6 nm) nitride/oxide gate stacks with bottom oxide materials and post-deposition treatment. *IEEE Transactions on Electron Devices*, **2001**, 48, 2769-2776	2.9	1
9	Thermally-enhanced remote plasma nitrided ultrathin (1.65 nm) gate oxide with excellent performances in reduction of leakage current and boron diffusion. *IEEE Electron Device Letters*, **2001**, 22, 378-380	4.4	18
8	Improvement of junction leakage of nickel silicided junction by a Ti-capping layer. *IEEE Electron Device Letters*, **1999**, 20, 572-573	4.4	39
7	Direct determination of interface and bulk traps in stacked HfO/sub 2/ dielectrics using charge pumping method		2
6	Low power device technology with SiGe channel, HfSiON, and poly-Si gate		5
5	Electrical performance improvement in SiO/sub 2//HfSiO high-k gate stack for advanced low power device application		1
4	Conventional n-channel MOSFET devices using single layer HfO/sub 2/ and ZrO/sub 2/ as high-k gate dielectrics with polysilicon gate electrode		7
3	Two-dimensional materials for artificial synapses: toward a practical application. *Neuromorphic Computing and Engineering*,		1
2	Two-dimensional solid-phase crystallization toward centimeter-scale monocrystalline layered MoTe2via two-step annealing. *Journal of Materials Chemistry C*,	7.1	3
1	Giant Photoresponsivity and External Quantum Efficiency in a Contact-Engineered Broadband a-IGZO Phototransistor. *Advanced Functional Materials*,2200282	15.6	0