Tuo-Hung Hou

List of Publications by Year
in descending order

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163 papers	6,006 citations	136740 32 h-index	110170 64 g-index
164 all docs	164 docs citations	164 times ranked	8089 citing authors

#	Article	IF	Citations
1	SLIM: Simultaneous Logic-in-Memory Computing Exploiting Bilayer Analog OxRAM Devices. Scientific Reports, 2020, 10, 2567.	1.6	1,186
2	Recommended Methods to Study Resistive Switching Devices. Advanced Electronic Materials, 2019, 5, 1800143.	2.6	452
3	Origin of the threshold voltage instability in SiO2/HfO2 dual layer gate dielectrics. IEEE Electron Device Letters, 2003, 24, 87-89.	2.2	330
4	Electrode dependence of filament formation in HfO2 resistive-switching memory. Journal of Applied Physics, 2011, 109, .	1.1	261
5	Mitigating effects of non-ideal synaptic device characteristics for on-chip learning. , 2015, , .		165
6	Bipolar Nonlinear $hbox{Ni/TiO}_{2}hbox{/}hbox{Ni}$ Selector for 1S1R Crossbar Array Applications. IEEE Electron Device Letters, 2011, 32, 1427-1429.	2.2	163
7	Transition of stable rectification to resistive-switching in Ti/TiO2/Pt oxide diode. Applied Physics Letters, 2010, 96, .	1.5	154
8	Optically initialized robust valley-polarized holes in monolayer WSe2. Nature Communications, 2015, 6, 8963.	5.8	151
9	3D Ta/TaO_x/TiO₂/Ti synaptic array and linearity tuning of weight update for hardware neural network applications. Nanotechnology, 2016, 27, 365204.	1.3	150
10	Characterization and Modeling of Nonfilamentary Ta/TaOx/TiO2/Ti Analog Synaptic Device. Scientific Reports, 2015, 5, 10150.	1.6	148
11	Multi-level control of conductive nano-filament evolution in HfO₂ ReRAM by pulse-train operations. Nanoscale, 2014, 6, 5698-5702.	2.8	137
12	Standards for the Characterization of Endurance in Resistive Switching Devices. ACS Nano, 2021, 15, 17214-17231.	7.3	128
13	Dependence of Read Margin on Pull-Up Schemes in High-Density One Selectorâ€“One Resistor Crossbar Array. IEEE Transactions on Electron Devices, 2013, 60, 420-426.	1.6	127
14	Fully parallel write/read in resistive synaptic array for accelerating on-chip learning. Nanotechnology, 2015, 26, 455204.	1.3	109
15	One selector-one resistor (1S1R) crossbar array for high-density flexible memory applications. , 2011, , .		93
16	Mitigating Asymmetric Nonlinear Weight Update Effects in Hardware Neural Network Based on Analog Resistive Synapse. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 116-124.	2.7	87
17	Resistive random access memory (RRAM) technology: From material, device, selector, 3D integration to bottom-up fabrication. Journal of Electroceramics, 2017, 39, 21-38.	0.8	79
18	Homogeneous barrier modulation of TaO_x/TiO₂ bilayers for ultra-high endurance three-dimensional storage-class memory. Nanotechnology, 2014, 25, 165202.	1.3	76

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19	Design Optimization of Metal Nanocrystal Memoryâ€"Part I: Nanocrystal Array Engineering. IEEE Transactions on Electron Devices, 2006, 53, 3095-3102.	1.6	73
20	3D synaptic architecture with ultralow sub-10 fJ energy per spike for neuromorphic computation. , 2014, , .		73
21	Programmable Synaptic Metaplasticity and below Femtojoule Spiking Energy Realized in Graphene-Based Neuromorphic Memristor. ACS Applied Materials & Interfaces, 2018, 10, 20237-20243.	4.0	71
22	Largeâ€Area 2D Layered MoTe₂ by Physical Vapor Deposition and Solidâ€Phase Crystallization in a Telluriumâ€Free Atmosphere. Advanced Materials Interfaces, 2017, 4, 1700157.	1.9	61
23	Abnormal positive bias stress instability of Inâ€"Gaâ€"Znâ€"O thin-film transistors with low-temperature Al2O3 gate dielectric. Applied Physics Letters, 2016, 108, .	1.5	59
24	High-k gate stacks for planar, scaled CMOS integrated circuits. Microelectronic Engineering, 2003, 69, 152-167.	1.1	58
25	3D resistive RAM cell design for high-density storage class memoryâ€"a review. Science China Information Sciences, 2016, 59, 1.	2.7	54
26	Amorphous InGaZnO Thin-Film Transistors Compatible With Roll-to-Roll Fabrication at Room Temperature. IEEE Electron Device Letters, 2012, 33, 47-49.	2.2	48
27	Improvement of junction leakage of nickel silicided junction by a Ti-capping layer. IEEE Electron Device Letters, 1999, 20, 572-573.	2.2	46
28	Nonvolatile Memory With a Metal Nanocrystal/Nitride Heterogeneous Floating-Gate. IEEE Transactions on Electron Devices, 2005, 52, 2697-2702.	1.6	45
29	Evolution of RESET current and filament morphology in low-power HfO2 unipolar resistive switching memory. Applied Physics Letters, 2011, 98, .	1.5	43
30	High-Voltage Amorphous InGaZnO TFT With Al₂O₃High-<inline-formula> <tex-math notation="LaTeX">k </tex-math> </inline-formula> Dielectric for Low-Temperature Monolithic 3-D Integration. IEEE Transactions on Electron Devices, 2016, 63, 3944-3949.	1.6	41
31	Bipolar ${m Ni}/{m TiO}_{2}/{m HfO}_{2}/{m Ni}$ RRAM With Multilevel States and Self-Rectifying Characteristics. IEEE Electron Device Letters, 2013, 34, 885-887.	2.2	39
32	Statistical Model and Rapid Prediction of RRAM SET Speedâ€"Disturb Dilemma. IEEE Transactions on Electron Devices, 2013, 60, 3760-3766.	1.6	38
33	High-Performance Double-Gate $alpha $ -InGaZnO ISFET pH Sensor Using a HfO2 Gate Dielectric. IEEE Transactions on Electron Devices, 2018, 65, 237-242.	1.6	38
34	Design and optimization methodology for 3D RRAM arrays. , 2013, , .		36
35	Large-area few-layer MoS₂deposited by sputtering. Materials Research Express, 2016, 3, 065007.	0.8	34
36	Sub-nA Low-Current HZO Ferroelectric Tunnel Junction for High-Performance and Accurate Deep Learning Acceleration. , 2019, , .		34

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37	Effect of polycrystalline-silicon gate types on the opposite flatband voltage shift in n-type and p-type metalâ€“oxideâ€“semiconductor field-effect transistors for high-k-HfO2 dielectric. Applied Physics Letters, 2003, 83, 308-310.	1.5	33
38	Fabrication and Characterization of High-k Dielectric Nickel Titanate Thin Films Using a Modified Sol-Gel Method. Journal of the American Ceramic Society, 2011, 94, 250-254.	1.9	33
39	Integration of Self-Assembled Redox Molecules in Flash Memory Devices. IEEE Transactions on Electron Devices, 2011, 58, 826-834.	1.6	33
40	Ferroelectric HfZrO₂ With Electrode Engineering and Stimulation Schemes as Symmetric Analog Synaptic Weight Element for Deep Neural Network Training. IEEE Transactions on Electron Devices, 2020, 67, 4201-4207.	1.6	33
41	Design Optimization of Metal Nanocrystal Memoryâ€”Part II: Gate-Stack Engineering. IEEE Transactions on Electron Devices, 2006, 53, 3103-3109.	1.6	32
42	Crossbar array of selector-less TaOx/TiO2 bilayer RRAM. Microelectronics Reliability, 2015, 55, 2220-2223.	0.9	32
43	A Fluorographeneâ€Based Synaptic Transistor. Advanced Materials Technologies, 2019, 4, 1900422.	3.0	30
44	Conventional n-channel MOSFET devices using single layer HfO/sub 2/ and ZrO/sub 2/ as high-k gate dielectrics with polysilicon gate electrode. , 0, , .		29
45	Asymmetric electric field enhancement in nanocrystal memories. IEEE Electron Device Letters, 2005, 26, 879-881.	2.2	28
46	Flexible One Diodeâ€“One Resistor Crossbar Resistive-Switching Memory. Japanese Journal of Applied Physics, 2012, 51, 04DD09.	0.8	28
47	1-V Full-Swing Depletion-Load a-Inâ€“Gaâ€“Znâ€“O Inverters for Back-End-of-Line Compatible 3D Integration. IEEE Electron Device Letters, 2016, 37, 441-444.	2.2	27
48	Interface engineered HfO₂-based 3D vertical ReRAM. Journal Physics D: Applied Physics, 2016, 49, 215102.	1.3	26
49	Challenges and opportunities toward online training acceleration using RRAM-based hardware neural network. , 2017, , .		26
50	Polymorphism Control of Layered MoTe2 through Two-Dimensional Solid-Phase Crystallization. Scientific Reports, 2019, 9, 8810.	1.6	26
51	Progress and Benchmark of Spiking Neuron Devices and Circuits. Advanced Intelligent Systems, 2021, 3, 2100007.	3.3	26
52	Subnanometer Scaling of HfO[sub 2]/Metal Electrode Gate Stacks. Electrochemical and Solid-State Letters, 2004, 7, G164.	2.2	23
53	Fermi-Level Pinning in Nanocrystal Memories. IEEE Electron Device Letters, 2007, 28, 103-106.	2.2	22
54	Reversible transition of resistive switching induced by oxygen-vacancy and metal filaments in HfO2. Solid-State Electronics, 2013, 89, 167-170.	0.8	22

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55	A Comprehensive Modeling Framework for Ferroelectric Tunnel Junctions. , 2019, , .		22
56	Thermally-enhanced remote plasma nitrided ultrathin (1.65 nm) gate oxide with excellent performances in reduction of leakage current and boron diffusion. IEEE Electron Device Letters, 2001, 22, 378-380.	2.2	21
57	SIMS depth profiling of advanced gate dielectric materials. Applied Surface Science, 2003, 203-204, 409-413.	3.1	20
58	NV-BNN. , 2019, , .		20
59	Local Modulation of Electrical Transport in 2D Layered Materials Induced by Electron Beam Irradiation. ACS Applied Electronic Materials, 2019, 1, 684-691.	2.0	20
60	Flexible One Diodeâ€“One Resistor Crossbar Resistive-Switching Memory. Japanese Journal of Applied Physics, 2012, 51, 04DD09.	0.8	19
61	Rapid Prediction of RRAM RESET-State Disturb by Ramped Voltage Stress. IEEE Electron Device Letters, 2012, 33, 597-599.	2.2	19
62	Switching Mode and Mechanism in Binary Oxide Resistive Random Access Memory Using Ni Electrode. Japanese Journal of Applied Physics, 2013, 52, 031801.	0.8	19
63	Bilayer-Based Antiferroelectric HfZrO₂ Tunneling Junction With High Tunneling Electroresistance and Multilevel Nonvolatile Memory. IEEE Electron Device Letters, 2021, 42, 1464-1467.	2.2	19
64	Flexible Three-Bit-Per-Cell Resistive Switching Memory Using a-IGZO TFTs. IEEE Electron Device Letters, 2013, 34, 1265-1267.	2.2	18
65	Low-Voltage InGaZnO Ion-Sensitive Thin-Film Transistors Fabricated by Low-Temperature Process. IEEE Transactions on Electron Devices, 2016, 63, 5060-5063.	1.6	18
66	Bi₂O₂Se-Based True Random Number Generator for Security Applications. ACS Nano, 2022, 16, 6847-6857.	7.3	18
67	Programable molecular orbital states of C60 from integrated circuits. Applied Physics Letters, 2006, 89, 253113.	1.5	17
68	Diamond-shaped Ge and Ge0.9Si0.1 gate-all-around nanowire FETs with four {111} facets by dry etch technology. , 2015, , .		17
69	Categorization of Multilevel-Cell Storage-Class Memory: An RRAM Example. IEEE Transactions on Electron Devices, 2015, 62, 2510-2516.	1.6	16
70	Bi₂O₂Se-Based Memristor-Aided Logic. ACS Applied Materials & Interfaces, 2021, 13, 15391-15398.	4.0	16
71	RRAM SET speed-disturb dilemma and rapid statistical prediction methodology. , 2012, , .		15
72	Extremely Compact Integrate-and-Fire STT-MRAM Neuron: A Pathway toward All-Spin Artificial Deep Neural Network. , 2019, , .		15

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73	Giant Photoresponsivity and External Quantum Efficiency in a Contactâ€Engineered Broadband aâ€IGZO Phototransistor. Advanced Functional Materials, 2022, 32, .	7.8	14
74	Effective N-methyl-2-pyrrolidone wet cleaning for fabricating high-performance monolayer MoS2 transistors. Nano Research, 2019, 12, 303-308.	5.8	13
75	2D Materialsâ€Based Static Randomâ€Access Memory. Advanced Materials, 2022, 34, e2107894.	11.1	12
76	Characterization of high-k gate dielectric and metal gate electrode semiconductor samples with a total reflection X-ray fluorescence spectrometer. Spectrochimica Acta, Part B: Atomic Spectroscopy, 2004, 59, 1227-1234.	1.5	11
77	Stability of La₂O₃ Metalâ€“Insulatorâ€“Metal Capacitors under Constant Voltage Stress. Japanese Journal of Applied Physics, 2010, 49, 04DB16.	0.8	11
78	3D vertical TaO<inf>x</inf>/TiO<inf>2</inf> RRAM with over 10³ self-rectifying ratio and sub-μA operating current. , 2013, , .		11
79	Low power device technology with SiGe channel, HfSiON, and Poly-Si gate. , 0, , .		10
80	Optimizing Incremental Step Pulse Programming for RRAM Through Deviceâ€“Circuit Co-Design. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 617-621.	2.2	10
81	Nonvolatile memory with molecule-engineered tunneling barriers. Applied Physics Letters, 2008, 92, 153109.	1.5	9
82	Statistical Metrology of Metal Nanocrystal Memories With 3-D Finite-Element Analysis. IEEE Transactions on Electron Devices, 2009, 56, 1729-1735.	1.6	9
83	Dimensionally anisotropic graphene with high mobility and a high onâ€“off ratio in a three-terminal RRAM device. Materials Chemistry Frontiers, 2020, 4, 1756-1763.	3.2	9
84	Enhanced Electrostatics for Low-Voltage Operations in Nanocrystal Based Nanotube/Nanowire Memories. IEEE Nanotechnology Magazine, 2007, 6, 22-28.	1.1	8
85	32-nm Multigate Si-nTFET With Microwave-Annealed Abrupt Junction. IEEE Transactions on Electron Devices, 2016, 63, 1808-1813.	1.6	8
86	Redox Molecules for a Resonant Tunneling Barrier in Nonvolatile Memory. IEEE Transactions on Electron Devices, 2012, 59, 1189-1198.	1.6	7
87	Two-dimensional solid-phase crystallization toward centimeter-scale monocrystalline layered MoTe₂via two-step annealing. Journal of Materials Chemistry C, 2021, 9, 15566-15576.	2.7	7
88	Two-dimensional materials for artificial synapses: toward a practical application. Neuromorphic Computing and Engineering, 2022, 2, 012003.	2.8	7
89	Improved multi-level control of RRAM using pulse-train programming. , 2014, , .		6
90	Promising Engineering Approaches for Improving the Reliability of HfZrO_x 2-D and 3-D Ferroelectric Random Access Memories. IEEE Transactions on Electron Devices, 2020, 67, 5479-5483.	1.6	6

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91	Device quantization policy in variation-aware in-memory computing design. Scientific Reports, 2022, 12, 112.	1.6	6
92	Performance Enhancement and Transient Current Response of Ferroelectric Tunnel Junction: A Theoretical Study. IEEE Transactions on Electron Devices, 2022, 69, 4686-4692.	1.6	6
93	Dramatic reduction of gate leakage current in 1.61â€…nm HfO2 high-k dielectric poly-silicon gate with Al2O3 capping layer. Electronics Letters, 2002, 38, 1223.	0.5	5
94	Effective improvement of high-k Hf-silicateâ•silicon interface with thermal nitridation. Electronics Letters, 2003, 39, 421.	0.5	5
95	Neuromorphic pattern learning using HBM electronic synapse with excitatory and inhibitory plasticity. , 2015, , .		5
96	Suspended Diamond-Shaped Nanowire With Four {111} Facets for High-Performance Ge Gate-All-Around FETs. IEEE Transactions on Electron Devices, 2016, 63, 3837-3843.	1.6	5
97	Interchangeable Hebbian and Anti-Hebbian STDP Applied to Supervised Learning in Spiking Neural Network. , 2018, , .		5
98	Unipolar Parity of Ferroelectric-Antiferroelectric Characterized by Junction Current in Crystalline Phase Hf1â‾'xZrxO2 Diodes. Nanomaterials, 2021, 11, 2685.	1.9	5
99	Metal nanocrystal/nitride heterogeneous-stack floating gate memory. , 2005, , .		4
100	Flash Memory Scaling: From Material Selection to Performance Improvement. Materials Research Society Symposia Proceedings, 2008, 1071, 1.	0.1	4
101	Strong Read and Write Interference Induced by Breakdown Failure in Crossbar Arrays. IEEE Transactions on Electron Devices, 2020, 67, 5497-5504.	1.6	4
102	Low power nonvolatile SRAM circuit with integrated low voltage nanocrystal PMOS Flash. , 2010, , .		3
103	Novel Two-Bit-per-Cell Resistive-Switching Memory for Low-Cost Embedded Applications. IEEE Electron Device Letters, 2011, 32, 1662-1664.	2.2	3
104	Multi-bit-per-Cell a-IGZO TFT resistive-switching memory for system-on-plastic applications. , 2012, , .		3
105	On the potential of CRS, 1D1R, and 1S1R crossbar RRAM for storage-class memory. , 2013, , .		3
106	Stochastic STT-MRAM Spiking Neuron Circuit. , 2020, , .		3
107	Nonvolatile molecular memory with the multilevel states based on MoS₂ nanochannel field effect transistor through tuning gate voltage to control molecular configurations. Nanotechnology, 2020, 31, 275204.	1.3	3
108	TaOx-/TiO2-Based Synaptic Devices. , 2017, , 73-95.		3

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109	In-Memory Annealing Unit (IMAU): Energy-Efficient (2000 TOPS/W) Combinatorial Optimizer for Solving Travelling Salesman Problem. , 2021, , .		3
110	Improved current drivability and poly-gate depletion of submicron PMOSFET with poly-SiGe gate and ultra-thin nitride gate dielectric. Solid-State Electronics, 2002, 46, 597-599.	0.8	2
111	Direct determination of interface and bulk traps in stacked HfO/sub 2/ dielectrics using charge pumping method. , 0, , .		2
112	Three-dimensional analytical modeling of nanocrystal memory electrostatics. Journal of Applied Physics, 2006, 99, 114516.	1.1	2
113	Modeling of Multi-layer Nanocrystal Memory. Device Research Conference, IEEE Annual, 2007, , .	0.0	2
114	Strained Silicon Technology: Mobility Enhancement and Improved Short Channel Effect Performance by Stress Memorization Technique on nFET Devices. Journal of the Electrochemical Society, 2010, 157, H497.	1.3	2
115	Grain size and plasma doping effects on CVD-based 2D transition metal dichalcogenide. , 2016, , .		2
116	Pulse-Mediated Electronic Tuning of the MoS₂â€“Perovskite Ferroelectric Field Effect Transistors. ACS Applied Electronic Materials, 2020, 2, 3843-3852.	2.0	2
117	Hardware-Robust In-RRAM-Computing for Object Detection. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2022, 12, 547-556.	2.7	2
118	Base oxide scaling limit of thermally-enhanced remote plasma nitridation (TE-RPN) process for ultra-thin gate dielectric formation. , 0, , .		1
119	To optimize electrical properties of the ultrathin (1.6 nm) nitride/oxide gate stacks with bottom oxide materials and post-deposition treatment. IEEE Transactions on Electron Devices, 2001, 48, 2769-2776.	1.6	1
120	Spike anneal qualification for 0.13 Î¼m USJ technology on Radiance/spl trade/ Centura/spl reg/. , 0, , .		1
121	HfO2â^•HfSixOy high-K gate stack with very low leakage current for low-power poly-Si gated CMOS application. Electronics Letters, 2003, 39, 692.	0.5	1
122	Effects of base oxide in HfSiO/SiO/sub 2/ high-k gate stacks. , 0, , .		1
123	Electrical performance improvement in SiO/sub 2//HfSiO high-k gate stack for advanced low power device application. , 0, , .		1
124	Material and electrical characterization of stackable planar polysilicon TFT flash memory cell with metal nanocrystals and high-k dielectrics. , 2008, , .		1
125	Heterogeneous Integration of Molecules in Nonvolatile Memory. , 2008, , .		1
126	Low-I<inf>RESET</inf> unipolar HfO<inf>2</inf> RRAM and tunable resistive-switching mode via interface engineering. , 2011, , .		1

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127	Grain size effect of monolayer MoS2 transistors characterized by second harmonic generation mapping. , 2015, , .		1
128	A Study of Blocking and Tunnel Oxide Engineering on Double-Trapping (DT) BE-SONOS Performance. , 2015, , .		1
129	Reliable high-voltage amorphous InGaZnO TFT for monolithic 3D integration. , 2016, , .		1
130	Statistical study of RRAM MLC SET variability induced by filament morphology. , 2017, , .		1
131	AC stress and electronic effects on SET switching of HfO2 RRAM. Applied Physics Letters, 2017, 111, 093502.	1.5	1
132	Two-dimensional Layered Materials for Artificial Synapse. , 2020, , .		1
133	Semi-Empirical RC Circuit Model for Non-Filamentary Bi-Layer OxRAM Devices. IEEE Transactions on Electron Devices, 2020, 67, 1348-1352.	1.6	1
134	Exploiting analogue OxRAM conductance modulation for contrast enhancement application. Electronics Letters, 2020, 56, 594-597.	0.5	1
135	Resistive Random Access Memory (RRAM) Technology: From Material, Device, Selector, 3D Integration to Bottom-Up Fabrication. Kluwer International Series in Electronic Materials: Science and Technology, 2022, , 33-64.	0.3	1
136	An 1-bit by 1-bit High Parallelism In-RRAM Macro with Co-Training Mechanism for DCNN Applications. , 2022, , .		1
137	Ultrathin ox/nitride gate stack for sub-quarter-micron CMOS devices prepared by RTCVD. , 0, , .		0
138	Reliability studies of Hf-doped and NH3-nitrided gate dielectric for advanced CMOS application. IET Circuits, Devices and Systems, 2005, 152, 407.	0.6	0
139	3-D Electrostatic Modeling and Impact of High-κ Control Oxide in Metal Nanocrystal Memory. , 2006, , .		0
140	Effects of Metal Nanocrystals and Traps in Tunneling Rate Measurements in Metal Nanocrystal Based Carbon Nanotube Memory. Materials Research Society Symposia Proceedings, 2006, 963, 1.	0.1	0
141	Process Integration of Composite High-k Tunneling Dielectric for Nanocrystal Based Carbon Nanotube Memory. Materials Research Society Symposia Proceedings, 2006, 961, 1.	0.1	0
142	Planar polysilicon TFT low-voltage flash memory cell with Al<inf>2</inf>O<inf>3</inf> tunnel dielectric and (Ti,Dy) O control dielectric for three-dimensional integration. , 2008, , .		0
143	3D Finite-Element Analysis of Metal Nanocrystal Memories Variations. , 2009, , .		0
144	Room-temperature TiO<inf>x</inf> oxide diode for 1D1R resistance-switching memory. , 2009, , .		0

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145	Characterization of Highly Strained nFET Device Performance and Channel Mobility with SMT. Journal of the Electrochemical Society, 2010, 157, H705.	1.3	0
146	Improvement of polycrystalline silicon thin-film transistors with nickel-titanium oxide by sol-gel spin-coating and nitrogen implantation. , 2011, , .		0
147	High-performance Ni/SiO<inf>2</inf>/Si programmable metallization cell. , 2011, , .		0
148	Stackable nonvolatile memory with ultra thin polysilicon film and low-leakage (Ti,Dy)xOy for low processing temperature and low operating voltages. Microelectronic Engineering, 2011, 88, 3462-3465.	1.1	0
149	Polycrystalline silicon thin-film transistor with nickelâ€“titanium oxide by solâ€“gel spin-coating and nitrogen implantation. Solid-State Electronics, 2012, 78, 11-16.	0.8	0
150	Logic/resistive-switching hybrid transistor for two-bit-per-cell storage. , 2012, , .		0
151	Fast visible-light phototransistor using CVD-synthesized large-area bilayer WSe<inf>2</inf>. , 2014, , .		0
152	Investigating MLC variation of filamentary and non-filamentary RRAM. , 2014, , .		0
153	Development of three-dimensional synaptic device and neuromorphic computing hardware. , 2016, , .		0
154	Suspended Ge gate-all-around nanowire nFETs with junction isolation on bulk Si. , 2016, , .		0
155	Internal current amplification induced by dielectric hole trapping in monolayer MoS2 transistor. Nanotechnology, 2017, 28, 475204.	1.3	0
156	High-conductance Two-dimensional 1T'-MoTe<inf>2</inf>Synthesized by Sputtering. , 2018, , .		0
157	Memristive devices by ALD: design aspects for high density 3D arrays for memory and neuromorphic applications. , 2018, , .		0
158	Three dimensional integration of ReRAMs. , 2018, , .		0
159	Study of Thyristor-Mode Dual-Channel NAND Flash Devices. , 2018, , .		0
160	Phase and Carrier Polarity Control of Sputtered MoTe2 by Plasma-induced Defect Engineering. , 2020, , .		0
161	Drain-Bias Transient Instability of Amorphous Indiumâ€“Galliumâ€“Zinc Oxide Thin-Film Transistors. IEEE Transactions on Electron Devices, 2020, 67, 4526-4529.	1.6	0
162	Strategy of Mitigating Breakdown Interference and Yield Loss in Crossbar Memory. IEEE Transactions on Electron Devices, 2021, 68, 6082-6086.	1.6	0

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163	Voltageâ€“Time Transformation Model for Threshold Switching Spiking Neuron Based on Nucleation Theory. Frontiers in Neuroscience, 2022, 16, 868671.	1.4	0