Hui Pan

List of Publications by Year
in descending order

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14 papers	368 citations	1307594 7 h-index	1588992 8 g-index
14 all docs	14 docs citations	14 times ranked	238 citing authors

#	Article	IF	Citations
1	A 3.3-V 12-b 50-MS/s A/D converter in 0.6-/spl mu/m CMOS with over 80-dB SFDR. IEEE Journal of Solid-State Circuits, 2000, 35, 1769-1780.	5.4	92
2	A 500 mW ADC-Based CMOS AFE With Digital Calibration for 10 Gb/s Serial Links Over KR-Backplane and Multimode Fiber. IEEE Journal of Solid-State Circuits, 2010, 45, 1172-1185.	5.4	62
3	Signal Folding in A/D Converters. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 3-14.	0.1	51
4	Spatial filtering in flash A/D converters. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2003, 50, 424-436.	2.2	50
5	A New Class of Heterocyclic Compounds for Nonlinear Optics. Chemistry of Materials, 1995, 7, 816-821.	6.7	47
6	Spectral Spurs due to Quantization in Nyquist ADCs. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 1422-1439.	0.1	37
7	A Full-Duplex Line Driver for Gigabit Ethernet With Rail-to-Rail Class-AB Output Stage in 28 nm CMOS. IEEE Journal of Solid-State Circuits, 2014, 49, 3141-3155.	5.4	13
8	A digital wideband CDR with ±15.6kppm frequency tracking at 8Gb/s in 40nm CMOS. , 2011, , .		5
9	A 3.3 V, 12b, 50MSample/s A/D converter in 0.6 Î¼m CMOS with over 80 dB SFDR. , 0, , .		4
10	A 3.3-V 12b 50-MS/s A/D Converter in 0.6-Âµm CMOS with over 80-dB SFDR. , 2000, , 47-73.		2
11	8.6 A full-duplex line driver for Gigabit Ethernet with rail-to-rail class-AB output stage in 28nm CMOS. , 2014, , .		2
12	A dual-residue pipelined SAR ADC using only zero-crossing signals. Analog Integrated Circuits and Signal Processing, 2021, 108, 229-239.	1.4	2
13	10.3 An analog front-end for 100BASE-T1 automotive Ethernet in 28nm CMOS. , 2016, , .		1
14	A/D converter fundamentals and trends. , 2017, , .		0