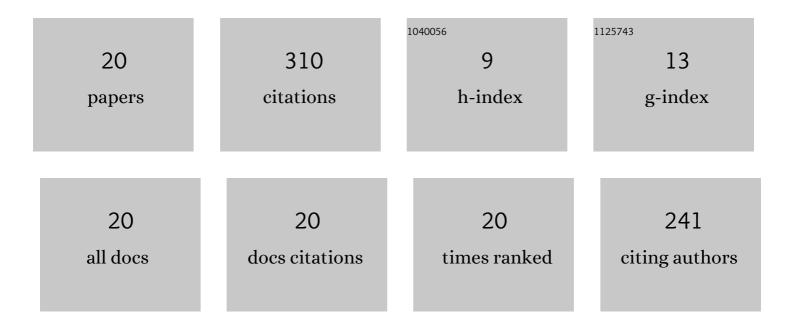
Wonbo Shim

List of Publications by Year in descending order

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WONRO SHIM

#	Article	IF	CITATIONS
1	Temperature-Resilient RRAM-Based In-Memory Computing for DNN Inference. IEEE Micro, 2022, 42, 89-98.	1.8	6
2	A Technology Path for Scaling Embedded FeRAM to 28 nm and Beyond With 2T1C Structure. IEEE Transactions on Electron Devices, 2022, 69, 109-114.	3.0	5
3	GP3D: 3D NAND Based In-Memory Graph Processing Accelerator. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2022, 12, 500-507.	3.6	4
4	Sparse and Robust RRAM-based Efficient In-memory Computing for DNN Inference. , 2022, , .		1
5	Technological Design of 3D NAND-Based Compute-in-Memory Architecture for GB-Scale Deep Neural Network. IEEE Electron Device Letters, 2021, 42, 160-163.	3.9	31
6	Characterization and Mitigation of Relaxation Effects on Multi-level RRAM based In-Memory Computing. , 2021, , .		6
7	Impact of Multilevel Retention Characteristics on RRAM based DNN Inference Engine. , 2021, , .		9
8	Impact of Random Phase Distribution in Ferroelectric Transistors-Based 3-D NAND Architecture on In-Memory Computing. IEEE Transactions on Electron Devices, 2021, 68, 2543-2548.	3.0	15
9	System-Technology Codesign of 3-D NAND Flash-Based Compute-in-Memory Inference Engine. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, 7, 61-69.	1.5	6
10	Ferroelectric Field-Effect Transistor-Based 3-D NAND Architecture for Energy-Efficient on-Chip Training Accelerator. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, 7, 1-9.	1.5	10
11	RRAM for Compute-in-Memory: From Inference to Training. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2753-2765.	5.4	46
12	Ferroelectric HfO ₂ -based synaptic devices: recent trends and prospects. Semiconductor Science and Technology, 2021, 36, 104001.	2.0	25
13	Compute-in-Memory: From Device Innovation to 3D System Integration. , 2021, , .		5
14	Impact of Read Disturb on Multilevel RRAM based Inference Engine: Experiments and Model Prediction. , 2020, , .		18
15	Investigation of Read Disturb and Bipolar Read Scheme on Multilevel RRAM-Based Deep Learning Inference Engine. IEEE Transactions on Electron Devices, 2020, 67, 2318-2323.	3.0	28
16	Drain–Erase Scheme in Ferroelectric Field-Effect Transistor—Part I: Device Characterization. IEEE Transactions on Electron Devices, 2020, 67, 955-961.	3.0	26
17	Drain-Erase Scheme in Ferroelectric Field Effect Transistor—Part II: 3-D-NAND Architecture for In-Memory Computing. IEEE Transactions on Electron Devices, 2020, 67, 962-967.	3.0	29
18	Architectural Design of 3D NAND Flash based Compute-in-Memory for Inference Engine. , 2020, , .		7

#	Article	IF	CITATIONS
19	Impact of Random Phase Distribution in 3D Vertical NAND Architecture of Ferroelectric Transistors on In-Memory Computing. , 2020, , .		5
20	Two-step write–verify scheme and impact of the read noise in multilevel RRAM-based inference engine. Semiconductor Science and Technology, 2020, 35, 115026.	2.0	28