Tai-Cheng Lee

List of Publications by Year
in descending order

49 papers	643 citations	687363 13 h-index	794594 19 g-index
49 all docs	49 docs citations	49 times ranked	615 citing authors

#	Article	IF	Citations
1	A Fractional-N Divider-Less Phase-Locked Loop With a Subsampling Phase Detector. IEEE Journal of Solid-State Circuits, 2014, 49, 2964-2975.	5.4	110
2	The Design and Analysis of Dual-Delay-Path Ring Oscillators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 470-478.	5.4	69
3	The Design and Analysis of a DLL-Based Frequency Synthesizer for UWB Application. IEEE Journal of Solid-State Circuits, 2006, 41, 1245-1252.	5.4	55
4	A 10-bit 2.6-GS/s Time-Interleaved SAR ADC With a Digital-Mixing Timing-Skew Calibration Technique. IEEE Journal of Solid-State Circuits, 2018, 53, 1508-1517.	5.4	53
5	A stabilization technique for phase-locked frequency synthesizers. IEEE Journal of Solid-State Circuits, 2003, 38, 888-894.	5.4	52
6	A 6-bit 800-MS/s Pipelined A/D Converter With Open-Loop Amplifiers. IEEE Journal of Solid-State Circuits, 2007, 42, 258-268.	5.4	28
7	A 10-bit 100-MS/s 4.5-mW Pipelined ADC With a Time-Sharing Technique. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 1157-1166.	5.4	28
8	A mixed-signal GFSK demodulator for Bluetooth. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 197-201.	2.2	26
9	A Split-Based Digital Background Calibration Technique in Pipelined ADCs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 855-859.	3.0	25
10	A 12-bit 210-MS/s 2-Times Interleaved Pipelined-SAR ADC With a Passive Residue Transfer Technique. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 929-938.	5.4	24
11	An 8-GHz to 10-GHz Distributed DLL for Multiphase Clock Generation. IEEE Journal of Solid-State Circuits, 2009, 44, 2478-2487.	5.4	22
12	A 0.02-mm^{2} 9-Bit 50-MS/s Cyclic ADC in 90-nm Digital CMOS Technology. IEEE Journal of Solid-State Circuits, 2010, 45, 610-619.	5.4	20
13	The Study of a Dual-Mode Ring Oscillator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 210-214.	3.0	16
14	Efficient Heat Dissipation of Uncooled 400-Gbps (16Ã—25-Gbps) Optical Transceiver Employing Multimode VCSEL and PD Arrays. Scientific Reports, 2017, 7, 46608.	3.3	13
15	The Design and Analysis of a Fully Integrated Multiplying DLL With Adaptive Current Tuning. IEEE Journal of Solid-State Circuits, 2008, 43, 1427-1435.	5.4	11
16	Nonlinear R-2R Transistor-Only DAC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2644-2653.	5.4	9
17	A 5 GHz Fractional-<inline-formula> <tex-math notation="LaTeX">N</tex-math> </inline-formula> ADC-Based Digital Phase-Locked Loops With â^'243.8 dB FOM. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1845-1853.	5.4	9
18	A DLL-based frequency multiplier for MBOA-UWB system. , 0, , .		8

#	Article	IF	Citations
19	A 40-GHz Distributed-Load Static Frequency Divider. , 2005, , .		8
20	The Design and Analysis of a Miller-Divider-Based Clock Generator for MBOA-UWB Application. IEEE Journal of Solid-State Circuits, 2006, 41, 1253-1261.	5.4	8
21	An 833-MHz 132-phase multiphase clock generator with self-calibration circuits. , 2008, , .		6
22	An all-digital de-skew clock generator for arbitrary wide range delay. , 2010, , .		5
23	A 10-bit binary-weighted DAC with digital background LMS calibration. , 2007, , .		4
24	A 6-bit pipelined analog-to-digital converter with current-switching open-loop residue amplification. , 2008, , .		4
25	A 4-PAM adaptive analog equalizer for backplane interconnections. , 2008, , .		4
26	An Optimization Technique for RF Buffers with Active Inductors. , 0, , .		3
27	A 14-Gb/s 4-PAM Adaptive Analog Equalizer for 40-inch Backplane Interconnections. , 2006, , .		3
28	A Fully Integrated 36MHz to 230MHz Multiplying DLL with Adaptive Current Tuning. , 2007, , .		3
29	Ultraâ€lowâ€power oneâ€pin crystal oscillator with selfâ€charged technique. Electronics Letters, 2016, 52, 325-327.	1.0	3
30	A 10 Gbase-LX4 receiver front end transimpedance amplifier and limiting amplifier. , 0, , .		2
31	A Linear-Approximation Technique for Digitally-Calibrated Pipelined A/D Converters. , 0, , .		2
32	A 10-Gb/s equalizer with digital adaptation. , 2017, , .		2
33	An 8-bit 2-V 2-mW 0.25-mm/sup 2/ CMOS DAC. , 0, , .		1
34	High-precision frequency synthesizers for UWB applications. , 0, , .		1
35	A 4-Channel Poly-Phase Filter for Cognitive Radio Systems. , 2007, , .		1
36	A clock and data recovery circuit with wide linear range frequency detector. , 2008, , .		1

#	Article	IF	Citations
37	An offset phase-locked loop spread spectrum clock generator for SATA III. , 2010, , .		1
38	A 10-bit 400-MS/s 36-mW interleaved ADC. , 2011, , .		1
39	A 3X-oversampling hybrid clock and data recovery circuit with programmable bandwidth. , 2014, , .		1
40	A 5.12-GHz fractional-N frequency synthesizer with an LC-VCO-based MDLL. , 2017, , .		1
41	CMOS 2.4-GHz receiver front end with area-efficient inductors and digitally calibrated 90Â° delay network. , 0, , .		0
42	A 6-bit 500-Ms/s digital self-calibrated pipelined analog-to-digital converter. , 0, , .		0
43	A 300- to 800-MHz de-skew clock generator for arbitrary delay. , 2010, , .		0
44	A 10-bit piplined A/D converter with split calibration and opamp-sharing technique. , 2010, , .		0
45	A 10-bit 200-MS/s reconfigurable pipelined A/D converter. , 2012, , .		0
46	Jitter error cancellation technique in digital domain for ADC. , 2013, , .		0
47	Analysis of the leakage effect in a pipelined ADC with nanoscale CMOS technologies. , 2013, , .		0
48	A Wireline Termination Embedded Energy Harvesting System With 300-Î¼W Extracted. IEEE Solid-State Circuits Letters, 2020, 3, 438-441.	2.0	0
49	A Single-Channel 1-GS/s 7.48-ENOB Parallel Conversion Pipelined SAR ADC With a Varactor-Based Residue Amplifier. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2021-2025.	3.0	0