

Federico Pepe

List of Publications by Year in descending order

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papers

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20
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248
citing authors

#	ARTICLE	IF	CITATIONS
1	Suppression of Flicker Noise Up-Conversion in a 65-nm CMOS VCO in the 3.0-to-3.6 GHz Band. IEEE Journal of Solid-State Circuits, 2013, 48, 2375-2389.	3.5	75
2	Analysis and Minimization of Flicker Noise Up-Conversion in Voltage-Biased Oscillators. IEEE Transactions on Microwave Theory and Techniques, 2013, 61, 2382-2394.	2.9	57
3	Flicker Noise Up-Conversion due to Harmonic Distortion in Van der Pol CMOS Oscillators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1418-1430.	3.5	40
4	Efficient Calculation of the Impulse Sensitivity Function in Oscillators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 628-632.	2.2	27
5	A General Theory of Phase Noise in Transconductor-Based Harmonic Oscillators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 432-445.	3.5	27
6	Analysis of a 28-nm CMOS Fast-Lock Bang-Bang Digital PLL With 220-fs RMS Jitter for Millimeter-Wave Communication. IEEE Journal of Solid-State Circuits, 2020, 55, 1854-1863.	3.5	25
7	An efficient linear-time variant simulation technique of oscillator phase sensitivity function. , 2012, , .		19
8	An Accurate Analysis of Phase Noise in CMOS Ring Oscillators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1292-1296.	2.2	18
9	A Unified Method for the Analysis of Phase and Amplitude Noise in Electrical Oscillators. IEEE Transactions on Microwave Theory and Techniques, 2013, 61, 3277-3284.	2.9	14
10	Still More on the $\frac{1}{f^2}$ Phase Noise Performance of Harmonic Oscillators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 538-542.	2.2	8
11	An experimental comparison between two widely adopted phase noise models. , 2016, , .		7
12	On the Remarkable Performance of the Series-Resonance CMOS Oscillator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 531-542.	3.5	7
13	A 22.5-27.7-GHz Fast-Lock Bang-Bang Digital PLL in 28-nm CMOS for Millimeter-Wave Communication With 220-fs RMS Jitter. IEEE Solid-State Circuits Letters, 2019, 2, 111-114.	1.3	7
14	A 23 GHz Low-Phase-Noise Transformer-Feedback VCO in 22nm FD-SOI with a FOMT of 191dBc/Hz. , 2018, , .		6
15	Simulating phase noise induced from cyclostationary noise sources. , 2013, , .		4
16	40GHz Frequency Tripler with High Fundamental and Harmonics Rejection in 55nm SiGe-BiCMOS. , 2019, , .		3
17	A 2.8-3.8-GHz Low-Spur DTC-Based DPLL With a Class-D DCO in 65-nm CMOS. IEEE Microwave and Wireless Components Letters, 2017, 27, 1010-1012.	2.0	2
18	Impact of non-quasi-static effects on $1/f^3$ phase noise in a 1.9-to-2.6 GHz oscillator. , 2014, , .		1

#	ARTICLE	IF	CITATIONS
19	Reducing flicker noise up-conversion in a 65nm CMOS VCO in the 1.6 to 2.6 GHz band. Proceedings of SPIE, 2013, , .	0.8	0
20	A simulation technique to compute phase noise induced from cyclostationary noise sources in RF oscillators. Proceedings of SPIE, 2013, , .	0.8	0