# Pasquale Corsonello

## List of Publications by Year in Descending Order



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|---|---|---|---|
| 116 papers | 1,146 citations | 16 h-index | 27 g-index |
| 132 ext. papers | 1,527 ext. citations | 2 avg, IF | 4.59 L-index |

| # | Paper | IF | Citations |
|---|---|---|---|
| 116 | Approximate Down-Sampling Strategy for Power-Constrained Intelligent Systems. *IEEE Access*, **2022**, 1-1 | 3.5 | 0 |
| 115 | Robust and High-Performance Machine Vision System for Automatic Quality Inspection in Assembly Processes.. *Sensors*, **2022**, 22, | 3.8 | 2 |
| 114 | Aggressive Approximation of the SoftMax Function for Power-Efficient Hardware Implementations. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 1-1 | 3.5 | 1 |
| 113 | Accuracy Improved Low-Energy Multi-bit Approximate Adders in QCA. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 1-1 | 3.5 | 1 |
| 112 | Approximate Multipliers With Dynamic Truncation for Energy Reduction via Graceful Quality Degradation. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 3427-3431 | 3.5 | 5 |
| 111 | Energy-Efficient Architecture for CNNs Inference on Heterogeneous FPGA. *Journal of Low Power Electronics and Applications*, **2020**, 10, 1 | 1.7 | 11 |
| 110 | A Parallel Connected Component Labeling Architecture for Heterogeneous Systems-on-Chip. *Electronics (Switzerland)*, **2020**, 9, 292 | 2.6 | 4 |
| 109 | Parallel architecture of power-of-two multipliers for FPGAs. *IET Circuits, Devices and Systems*, **2020**, 14, 381-389 | 1.1 | 5 |
| 108 | Efficient Approximate Adders for FPGA-Based Data-Paths. *Electronics (Switzerland)*, **2020**, 9, 1529 | 2.6 | 6 |
| 107 | Efficient Deconvolution Architecture for Heterogeneous Systems-on-Chip. *Journal of Imaging*, **2020** , 6, | 3.1 | 1 |
| 106 | Stereo vision architecture for heterogeneous systems-on-chip. *Journal of Real-Time Image Processing*, **2020**, 17, 393-415 | 1.9 | 5 |
| 105 | An embedded machine vision system for an in-line quality check of assembly processes. *Procedia Manufacturing*, **2020**, 42, 211-218 | 1.5 | 12 |
| 104 | Efficient Architecture for Integral Image Computation on Heterogeneous FPGAs **2019**, | | 2 |
| 103 | An Efficient Hardware-Oriented Single-Pass Approach for Connected Component Analysis. *Sensors*, **2019**, 19, | 3.8 | 8 |
| 102 | Automatic Microstructural Classification with Convolutional Neural Network. *Advances in Intelligent Systems and Computing*, **2019**, 170-181 | 0.4 | 2 |
| 101 | Energy-Quality Scalable Adders Based on Nonzeroing Bit Truncation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 964-968 | 2.6 | 10 |
| 100 | Multimodal background subtraction for high-performance embedded systems. *Journal of Real-Time Image Processing*, **2019**, 16, 1407-1423 | 1.9 | 7 |

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| 99 | An Efficient Connected Component Labeling Architecture for Embedded Systems. *Journal of Low Power Electronics and Applications*, **2018**, 8, 7 | 1.7 | 13 |
| 98 | Design of Real-Time FPGA-based Embedded System for Stereo Vision **2018**, | | 8 |
| 97 | **2018**, | | 2 |
| 96 | Designing Fast Convolutional Engines for Deep Learning Applications **2018**, | | 5 |
| 95 | Design of efficient QCA multiplexers. *International Journal of Circuit Theory and Applications*, **2016**, 44, 602-615 | 2 | 12 |
| 94 | Radial-Shaped Single Varactor-Tuned Phasing Line for Active Reflectarrays. *IEEE Transactions on Antennas and Propagation*, **2016**, 64, 3254-3259 | 4.9 | 17 |
| 93 | An efficient hardware-oriented stereo matching algorithm. *Microprocessors and Microsystems*, **2016**, 46, 21-33 | 2.4 | 9 |
| 92 | Power supply noise in accurate delay model for the sub-threshold domain. *The Integration VLSI Journal*, **2015**, 50, 127-136 | 1.4 | 1 |
| 91 | Low-Leakage SRAM Wordline Drivers for the 28-nm UTBB FDSOI Technology. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 3133-3137 | 2.6 | 10 |
| 90 | Fast and Wide Range Voltage Conversion in Multisupply Voltage Designs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 388-391 | 2.6 | 47 |
| 89 | A sub-1 V nanopower temperature-compensated sub-threshold CMOS voltage reference with 0.065%/V line sensitivity. *International Journal of Circuit Theory and Applications*, **2015**, 43, 421-426 | 2 | 4 |
| 88 | Exploring well configurations for voltage level converter design in 28 nm UTBB FDSOI technology **2015**, | | 2 |
| 87 | A layout strategy for low-power voltage level shifters in 28nm UTBB FDSOI technology **2015**, | | 2 |
| 86 | Embedded surveillance system using background subtraction and Raspberry Pi **2015**, | | 6 |
| 85 | . *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 1456-1464 | 3.9 | 16 |
| 84 | Area-Delay Efficient Binary Adders in QCA. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 1174-1179 | 2.6 | 43 |
| 83 | Design of Efficient Binary Comparators in Quantum-Dot Cellular Automata. *IEEE Nanotechnology Magazine*, **2014**, 13, 192-202 | 2.6 | 31 |
| 82 | A novel background subtraction method based on color invariants and grayscale levels **2014**, | | 4 |

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| 81 | Design of high-speed low-power parallel-prefix adder trees in nanometer technologies. *International Journal of Circuit Theory and Applications*, **2014**, 42, 731-743 | 2 | 4 |
| 80 | Analyzing noise robustness of wide fan-in dynamic logic gates under process variations. *International Journal of Circuit Theory and Applications*, **2014**, 42, 452-467 | 2 | 2 |
| 79 | Gate-level body biasing technique for high-speed sub-threshold CMOS logic gates. *International Journal of Circuit Theory and Applications*, **2014**, 42, 65-70 | 2 | 32 |
| 78 | Adaptive Census Transform: A novel hardware-oriented stereovision algorithm. *Computer Vision and Image Understanding*, **2013**, 117, 29-41 | 4.3 | 30 |
| 77 | Low-cost FPGA stereo vision system for real time disparity maps calculation. *Microprocessors and Microsystems*, **2012**, 36, 281-288 | 2.4 | 18 |
| 76 | Analytical Delay Model Considering Variability Effects in Subthreshold Domain. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2012**, 59, 168-172 | 3.5 | 25 |
| 75 | Energy-efficient single-clock-cycle binary comparator. *International Journal of Circuit Theory and Applications*, **2012**, 40, 237-246 | 2 | 9 |
| 74 | Low-Power Level Shifter for Multi-Supply Voltage Designs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2012**, 59, 922-926 | 3.5 | 54 |
| 73 | New Methodology for the Design of Efficient Binary Addition Circuits in QCA. *IEEE Nanotechnology Magazine*, **2012**, 11, 1192-1200 | 2.6 | 32 |
| 72 | Comparative analysis of yield optimized pulsed flip-flops. *Microelectronics Reliability*, **2012**, 52, 1679-1689 | 2.2 | 20 |
| 71 | Beam-Scanning Reflectarray Based on a Single Varactor-Tuned Element. *International Journal of Antennas and Propagation*, **2012**, 2012, 1-5 | 1.2 | 14 |
| 70 | Design of a reconfigurable reflectarray based on a varactor tuned element **2012**, | | 10 |
| 69 | Tapered-Vth Approach for Energy-Efficient CMOS Buffers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2011**, 58, 2698-2707 | 3.9 | 5 |
| 68 | . *IEEE Journal of Solid-State Circuits*, **2011**, 46, 465-474 | 5.5 | 164 |
| 67 | Design of Energy Aware Adder Circuits Considering Random Intra-Die Process Variations. *Journal of Low Power Electronics and Applications*, **2011**, 1, 97-108 | 1.7 | 7 |
| 66 | Efficient memory architecture for image processing. *International Journal of Circuit Theory and Applications*, **2011**, 39, 351-356 | 2 | 9 |
| 65 | Fast-squarer circuits using 3-bit-scan without overlapping bits. *International Journal of Circuit Theory and Applications*, **2011**, 39, 1037-1047 | 2 | |
| 64 | A self-hosting configuration management system to mitigate the impact of Radiation-Induced Multi-Bit Upsets in SRAM-based FPGAs **2010**, | | 9 |

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| 63 | Exploiting Self-Reconfiguration Capability to Improve SRAM-based FPGA Robustness in Space and Avionics Applications. *ACM Transactions on Reconfigurable Technology and Systems*, **2010**, 4, 1-22 | 2.7 | 8 |
| 62 | A new low-power high-speed single-clock-cycle binary comparator **2010**, | | 7 |
| 61 | A Low-Leakage Single-Ended 6T SRAM Cell **2010**, | | 2 |
| 60 | Impact of Process Variations on Flip-Flops Energy and Timing Characteristics **2010**, | | 13 |
| 59 | Efficient absolute difference circuits in Virtex-5 FPGAs **2010**, | | 4 |
| 58 | An Efficient and Low-Cost Design Methodology to Improve SRAM-Based FPGA Robustness in Space and Avionics Applications. *Lecture Notes in Computer Science*, **2009**, 74-84 | 0.9 | 4 |
| 57 | Low-power split-path data-driven dynamic logic. *IET Circuits, Devices and Systems*, **2009**, 3, 303-312 | 1.1 | 12 |
| 56 | Design-Space Exploration of Energy-Delay-Area Efficient Coarse-Grain Reconfigurable Datapath **2009**, | | 7 |
| 55 | New performance/power/area efficient, reliable full adder design **2009**, | | 6 |
| 54 | Designing High-Speed Adders in Power-Constrained Environments. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2009**, 56, 172-176 | 3.5 | 17 |
| 53 | Design and Evaluation of an Energy-Delay-Area Efficient Datapath for Coarse-Grain Reconfigurable Computing Systems. *Journal of Low Power Electronics*, **2009**, 5, 326-338 | 1.2 | 6 |
| 52 | A New Dynamic Logic Circuit Design for an Effective Trade-Off between Noise-Immunity, Performance and Energy Dissipation. *Lecture Notes in Computer Science*, **2009**, 277-286 | 0.9 | 2 |
| 51 | Energy Efficient Coarse-Grain Reconfigurable Array for Accelerating Digital Signal Processing. *Lecture Notes in Computer Science*, **2009**, 297-306 | 0.9 | |
| 50 | High-performance noise-tolerant circuit techniques for CMOS dynamic logic. *IET Circuits, Devices and Systems*, **2008**, 2, 537 | 1.1 | 16 |
| 49 | A high flexible Early-Late Gate bit synchronizer in FPGA-based software defined radios **2008**, | | 9 |
| 48 | Power-Efficient High Throughput Reconfigurable Datapath Design for Portable Multimedia Devices **2008**, | | 3 |
| 47 | Fast Low-Cost Implementation of Single-Clock-Cycle Binary Comparator. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2008**, 55, 1239-1243 | 3.5 | 20 |
| 46 | A matrix product accelerator for field programmable systems on chip. *Microprocessors and Microsystems*, **2008**, 32, 53-67 | 2.4 | 7 |

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| 45 | A programmable carrier phase independent symbol timing recovery circuit for QPSK/OQPSK signals. *Microprocessors and Microsystems*, **2008**, 32, 437-446 | 2.4 | 6 |
| 44 | A new noise-tolerant dynamic logic circuit design **2007**, | | 5 |
| 43 | VLSI implementations of efficient isotropic flexible 2D convolvers. *IET Circuits, Devices and Systems*, **2007**, 1, 263 | 1.1 | 6 |
| 42 | Parallel Multipliers using 3-Bit-Scan without Overlapping Bits **2007**, | | 1 |
| 41 | **2007**, | | 2 |
| 40 | A New Reconfigurable Coarse-Grain Architecture for Multimedia Applications **2007**, | | 14 |
| 39 | MORA: A New Coarse-Grain Reconfigurable Array for High Throughput Multimedia Processing **2007** , 159-168 | | 11 |
| 38 | SIMD MULTIPLIERS FOR ACCELERATING EMBEDDED PROCESSORS IN FPGAs. *Journal of Circuits, Systems and Computers*, **2006**, 15, 537-550 | 0.9 | 1 |
| 37 | SAD-Based Stereo Matching Circuit for FPGAs **2006**, | | 16 |
| 36 | An Efficient Bit-Detection and Timing Recovery Circuit for FPGAs **2006**, | | 5 |
| 35 | Techniques for Leakage Energy Reduction in Deep Submicrometer Cache Memories. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2006**, 14, 1238-1249 | 2.6 | 17 |
| 34 | Low bit rate image compression core for onboard space applications. *IEEE Transactions on Circuits and Systems for Video Technology*, **2006**, 16, 114-128 | 6.4 | 15 |
| 33 | Microprocessor-based FPGA implementation of SPIHT image compression subsystems. *Microprocessors and Microsystems*, **2005**, 29, 299-305 | 2.4 | 10 |
| 32 | A high-performance fully reconfigurable FPGA-based 2D convolution processor. *Microprocessors and Microsystems*, **2005**, 29, 381-391 | 2.4 | 28 |
| 31 | Efficient recursive multiply architecture for FPGAs. *Electronics Letters*, **2005**, 41, 1314 | 1.1 | 1 |
| 30 | Cost-effective low-power processor-in-memory-based reconfigurable datapath for multimedia applications **2005**, | | 6 |
| 29 | Efficient addition circuits for Modular design of processors-in-memory. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2005**, 52, 1557-1567 | | 4 |
| 28 | EFFICIENT RECONFIGURABLE MANCHESTER ADDERS FOR LOW-POWER MEDIA PROCESSING. *Journal of Circuits, Systems and Computers*, **2005**, 14, 57-63 | 0.9 | |

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| 27 | Fast Low-Power 64-Bit Modular Hybrid Adder. *Lecture Notes in Computer Science*, **2005**, 609-617 | 0.9 | |
| 26 | Fast and energy-efficient Manchester carry-bypass adders. *IET Circuits, Devices and Systems*, **2004**, 151, 497 | | 12 |
| 25 | Variable precision arithmetic circuits for FPGA-based multimedia processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2004**, 12, 995-999 | 2.6 | 9 |
| 24 | A high-speed energy-efficient 64-bit reconfigurable binary adder. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2003**, 11, 939-943 | 2.6 | 10 |
| 23 | An efficient self-timed adder realized using conventional CMOS standard cells. *International Journal of Electronics*, **2003**, 90, 413-422 | 1.2 | |
| 22 | Variable Precision Multipliers for FPGA-Based Reconfigurable Computing Systems. *Lecture Notes in Computer Science*, **2003**, 661-669 | 0.9 | 3 |
| 21 | 64-bit reconfigurable adder for low power media processing. *Electronics Letters*, **2002**, 38, 397 | 1.1 | 10 |
| 20 | VLSI circuits for low-power high-speed asynchronous addition. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2002**, 10, 608-613 | 2.6 | 4 |
| 19 | Tradeoffs in Digital Binary Adder Design: the effects of floorplanning, number of levels of metals, and supply voltage on performance and area. *Network Theory and Applications*, **2001**, 261-288 | | 1 |
| 18 | High performance mixed-logic asynchronous datapaths with overlapped execution circuits. *International Journal of Electronics*, **2000**, 87, 1193-1208 | 1.2 | 2 |
| 17 | Design of 3:1 multiplexer standard cell. *Electronics Letters*, **2000**, 36, 1994 | 1.1 | 1 |
| 16 | Area-time-power tradeoff in cellular arrays VLSI implementations. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2000**, 8, 614-624 | 2.6 | 2 |
| 15 | VLSI Implementation of a Low-Power High-Speed Self-Timed Adder. *Lecture Notes in Computer Science*, **2000**, 195-204 | 0.9 | 2 |
| 14 | High performance square rooting circuit using hybrid radix-2 adders. *Electronics Letters*, **1999**, 35, 185 | 1.1 | 1 |
| 13 | Hybrid carry-select statistical carry look-ahead adder. *Electronics Letters*, **1999**, 35, 549 | 1.1 | 2 |
| 12 | A new high performance circuit for statistical carry lookahead addition. *International Journal of Electronics*, **1999**, 86, 713-722 | 1.2 | 4 |
| 11 | High speed self-timed pipelined datapath for square rooting. *IET Circuits, Devices and Systems*, **1999**, 146, 16 | | 4 |
| 10 | Estimation of power dissipation for transmission lines in deep-submicrometer ULSI circuits. *Microwave and Optical Technology Letters*, **1999**, 22, 97-101 | 1.2 | |

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| 9 | High performance VLSI modules for division and square root. *Microprocessors and Microsystems*, **1998**, 22, 239-246 | 2.4 | 3 |
| 8 | Efficient VLSI implementation of statistical carry lookahead adder. *Electronics Letters*, **1998**, 34, 876 | 1.1 | 1 |
| 7 | CMOS buffer sizing for long on-chip interconnects. *Electronics Letters*, **1998**, 34, 1937 | 1.1 | 3 |
| 6 | Design and demonstration of high throughput square rooting circuit. *Electronics Letters*, **1996**, 32, 434 | 1.1 | 5 |
| 5 | An efficient wavelet image encoder for FPGA-based designs | | 4 |
| 4 | Low-cost fully reconfigurable data-path for FPGA-based multimedia processor | | 1 |
| 3 | A low-power sub-nanosecond standard-cells based adder | | 1 |
| 2 | FPGA implementation of Bayesian neural networks for a stand-alone predictor of pollutants concentration in the air | | 2 |
| 1 | A matrix product coprocessor for FPGA embedded soft processors | | 7 |