Pasquale Corsonello

List of Publications by Year
in descending order

130	1,736	331259 21	377514 34
papers	citations	h-index	g-index

132	132	132	1147
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A 2.6 nW, 0.45 V Temperature-Compensated Subthreshold CMOS Voltage Reference. IEEE Journal of Solid-State Circuits, 2011, 46, 465-474.	3.5	244
2	Low-Power Level Shifter for Multi-Supply Voltage Designs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 922-926.	2.2	84
3	Fast and Wide Range Voltage Conversion in Multisupply Voltage Designs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 388-391.	2.1	79
4	Area-Delay Efficient Binary Adders in QCA. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1174-1179.	2.1	55
5	New Methodology for the Design of Efficient Binary Addition Circuits in QCA. IEEE Nanotechnology Magazine, 2012, 11, 1192-1200.	1.1	44
6	Gateâ€level body biasing technique for highâ€speed subâ€threshold CMOS logic gates. International Journal of Circuit Theory and Applications, 2014, 42, 65-70.	1.3	44
7	Analytical Delay Model Considering Variability Effects in Subthreshold Domain. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 168-172.	2.2	39
8	A high-performance fully reconfigurable FPGA-based 2D convolution processor. Microprocessors and Microsystems, 2005, 29, 381-391.	1.8	38
9	Design of Efficient Binary Comparators in Quantum-Dot Cellular Automata. IEEE Nanotechnology Magazine, 2014, 13, 192-202.	1.1	38
10	Adaptive Census Transform: A novel hardware-oriented stereovision algorithm. Computer Vision and Image Understanding, 2013, 117, 29-41.	3.0	33
11	Fast Low-Cost Implementation of Single-Clock-Cycle Binary Comparator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 1239-1243.	2.2	31
12	Comparative analysis of yield optimized pulsed flip-flops. Microelectronics Reliability, 2012, 52, 1679-1689.	0.9	28
13	Techniques for Leakage Energy Reduction in Deep Submicrometer Cache Memories. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 1238-1249.	2.1	27
14	High-performance noise-tolerant circuit techniques for CMOS dynamic logic. IET Circuits, Devices and Systems, 2008, 2, 537.	0.9	26
15	Low-power split-path data-driven dynamic logic. IET Circuits, Devices and Systems, 2009, 3, 303-312.	0.9	26
16	Low bit rate image compression core for onboard space applications. IEEE Transactions on Circuits and Systems for Video Technology, 2006, 16, 114-128.	5.6	24
17	A New Reconfigurable Coarse-Grain Architecture for Multimedia Applications. , 2007, , .		24
18	Designing High-Speed Adders in Power-Constrained Environments. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 172-176.	2.2	23

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19	Low-cost FPGA stereo vision system for real time disparity maps calculation. Microprocessors and Microsystems, 2012, 36, 281-288.	1.8	23
20	Radial-Shaped Single Varactor-Tuned Phasing Line for Active Reflectarrays. IEEE Transactions on Antennas and Propagation, 2016, 64, 3254-3259.	3.1	22
21	An embedded machine vision system for an in-line quality check of assembly processes. Procedia Manufacturing, 2020, 42, 211-218.	1.9	22
22	Fast and energy-efficient Manchester carry-bypass adders. IET Circuits, Devices and Systems, 2004, 151, 497.	0.6	21
23	SAD-Based Stereo Matching Circuit for FPGAs. , 2006, , .		21
24	Energy-Quality Scalable Adders Based on Nonzeroing Bit Truncation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 964-968.	2.1	20
25	Cost-effective low-power processor-in-memory-based reconfigurable datapath for multimedia applications. , 2005, , .		19
26	Beam-Scanning Reflectarray Based on a Single Varactor-Tuned Element. International Journal of Antennas and Propagation, 2012, 2012, 1-5.	0.7	18
27	Over/Undershooting Effects in Accurate Buffer Delay Model for Sub-Threshold Domain. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1456-1464.	3.5	18
28	Energyâ€efficient singleâ€clockâ€cycle binary comparator. International Journal of Circuit Theory and Applications, 2012, 40, 237-246.	1.3	17
29	An Efficient Connected Component Labeling Architecture for Embedded Systems. Journal of Low Power Electronics and Applications, 2018, 8, 7.	1.3	17
30	A new low-power high-speed single-clock-cycle binary comparator. , 2010, , .		16
31	Impact of Process Variations on Flip-Flops Energy and Timing Characteristics. , 2010, , .		16
32	Design of a reconfigurable reflectarray based on a varactor tuned element. , 2012, , .		16
33	Energy-Efficient Architecture for CNNs Inference on Heterogeneous FPGA. Journal of Low Power Electronics and Applications, 2020, 10, 1.	1.3	16
34	A matrix product accelerator for field programmable systems on chip. Microprocessors and Microsystems, 2008, 32, 53-67.	1.8	15
35	Design of efficient QCA multiplexers. International Journal of Circuit Theory and Applications, 2016, 44, 602-615.	1.3	15
36	A high-speed energy-efficient 64-bit reconfigurable binary adder. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2003, 11, 939-943.	2.1	14

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37	Microprocessor-based FPGA implementation of SPIHT image compression subsystems. Microprocessors and Microsystems, 2005, 29, 299-305.	1.8	14
38	An Efficient Hardware-Oriented Single-Pass Approach for Connected Component Analysis. Sensors, 2019, 19, 3055.	2.1	14
39	64-bit reconfigurable adder for low power media processing. Electronics Letters, 2002, 38, 397.	0.5	13
40	A new noise-tolerant dynamic logic circuit design. , 2007, , .		13
41	Exploiting Self-Reconfiguration Capability to Improve SRAM-based FPGA Robustness in Space and Avionics Applications. ACM Transactions on Reconfigurable Technology and Systems, 2010, 4, 1-22.	1.9	13
42	Efficient Approximate Adders for FPGA-Based Data-Paths. Electronics (Switzerland), 2020, 9, 1529.	1.8	13
43	Approximate Multipliers With Dynamic Truncation for Energy Reduction via Graceful Quality Degradation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3427-3431.	2.2	13
44	Variable precision arithmetic circuits for FPGA-based multimedia processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2004, 12, 995-999.	2.1	12
45	A high flexible Early-Late Gate bit synchronizer in FPGA-based software defined radios. , 2008, , .		12
46	Design of Real-Time FPGA-based Embedded System for Stereo Vision. , 2018, , .		12
47	A self-hosting configuration management system to mitigate the impact of Radiation-Induced Multi-Bit Upsets in SRAM-based FPGAs. , 2010, , .		11
48	Efficient memory architecture for image processing. International Journal of Circuit Theory and Applications, 2011, 39, 351-356.	1.3	11
49	Low-Leakage SRAM Wordline Drivers for the 28-nm UTBB FDSOI Technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 3133-3137.	2.1	11
50	Stereo vision architecture for heterogeneous systems-on-chip. Journal of Real-Time Image Processing, 2020, 17, 393-415.	2.2	11
51	A programmable carrier phase independent symbol timing recovery circuit for QPSK/OQPSK signals. Microprocessors and Microsystems, 2008, 32, 437-446.	1.8	10
52	Design-Space Exploration of Energy-Delay-Area Efficient Coarse-Grain Reconfigurable Datapath. , 2009, , .		10
53	An efficient hardware-oriented stereo matching algorithm. Microprocessors and Microsystems, 2016, 46, 21-33.	1.8	10
54	Design and Evaluation of an Energy-Delay-Area Efficient Datapath for Coarse-Grain Reconfigurable Computing Systems. Journal of Low Power Electronics, 2009, 5, 326-338.	0.6	10

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55	A matrix product coprocessor for FPGA embedded soft processors. , 0, , .		9
56	New performance/power/area efficient, reliable full adder design. , 2009, , .		9
57	Design of Energy Aware Adder Circuits Considering Random Intra-Die Process Variations. Journal of Low Power Electronics and Applications, 2011, 1, 97-108.	1.3	9
58	Embedded surveillance system using background subtraction and Raspberry Pi. , 2015, , .		9
59	Design and demonstration of high throughput square rooting circuit. Electronics Letters, 1996, 32, 434.	0.5	8
60	Power-Efficient High Throughput Reconfigurable Datapath Design for Portable Multimedia Devices. , 2008, , .		8
61	Multimodal background subtraction for high-performance embedded systems. Journal of Real-Time Image Processing, 2019, 16, 1407-1423.	2.2	8
62	An Efficient Bit-Detection and Timing Recovery Circuit for FPGAs. , 2006, , .		7
63	An efficient and optimized FPGA Feedback M-PSK Symbol Timing Recovery Architecture based on the Gardner Timing Error Detector. , 2007, , .		7
64	An Efficient and Low-Cost Design Methodology to Improve SRAM-Based FPGA Robustness in Space and Avionics Applications. Lecture Notes in Computer Science, 2009, , 74-84.	1.0	7
65	Efficient absolute difference circuits in Virtex-5 FPGAs. , 2010, , .		7
66	Design of highâ€speed lowâ€power parallelâ€prefix adder trees in nanometer technologies. International Journal of Circuit Theory and Applications, 2014, 42, 731-743.	1.3	7
67	A Parallel Connected Component Labeling Architecture for Heterogeneous Systems-on-Chip. Electronics (Switzerland), 2020, 9, 292.	1.8	7
68	Parallel architecture of powerâ€ofâ€two multipliers for FPGAs. IET Circuits, Devices and Systems, 2020, 14, 381-389.	0.9	7
69	Aggressive Approximation of the SoftMax Function for Power-Efficient Hardware Implementations. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 1652-1656.	2.2	7
70	High speed self-timed pipelined datapath for square rooting. IET Circuits, Devices and Systems, 1999, 146, 16.	0.6	6
71	Area-time-power tradeoff in cellular arrays VLSI implementations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2000, 8, 614-624.	2.1	6
72	VLSI circuits for low-power high-speed asynchronous addition. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2002, 10, 608-613.	2.1	6

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73	Efficient addition circuits for Modular design of processors-in-memory. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2005, 52, 1557-1567.	0.1	6
74	VLSI implementations of efficient isotropic flexible 2D convolvers. IET Circuits, Devices and Systems, 2007, 1, 263.	0.9	6
75	Tapered-Vth Approach for Energy-Efficient CMOS Buffers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2698-2707.	3.5	6
76	Analyzing noise robustness of wide fanâ€in dynamic logic gates under process variations. International Journal of Circuit Theory and Applications, 2014, 42, 452-467.	1.3	6
77	Designing Fast Convolutional Engines for Deep Learning Applications. , 2018, , .		6
78	High performance VLSI modules for division and square root. Microprocessors and Microsystems, 1998, 22, 239-246.	1.8	5
79	Efficient VLSI implementation of statistical carry lookahead adder. Electronics Letters, 1998, 34, 876.	0.5	5
80	A low-power sub-nanosecond standard-cells based adder. , 0, , .		5
81	A novel background subtraction method based on color invariants and grayscale levels. , 2014, , .		5
82	A subâ€1â€‰V nanopower temperatureâ€compensated subâ€threshold CMOS voltage reference with 0.065%/V line sensitivity. International Journal of Circuit Theory and Applications, 2015, 43, 421-426.	1.3	5
83	Efficient Deconvolution Architecture for Heterogeneous Systems-on-Chip. Journal of Imaging, 2020, 6, 85.	1.7	5
84	Accuracy Improved Low-Energy Multi-Bit Approximate Adders in QCA. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3456-3460.	2.2	5
85	Approximate Down-Sampling Strategy for Power-Constrained Intelligent Systems. IEEE Access, 2022, 10, 7073-7081.	2.6	5
86	Robust and High-Performance Machine Vision System for Automatic Quality Inspection in Assembly Processes. Sensors, 2022, 22, 2839.	2.1	5
87	A new high performance circuit for statistical carry lookahead addition. International Journal of Electronics, 1999, 86, 713-722.	0.9	4
88	An efficient wavelet image encoder for FPGA-based designs. , 0, , .		4
89	A Low-Leakage Single-Ended 6T SRAM Cell. , 2010, , .		4
90	High performance mixed-logic asynchronous datapaths with overlapped execution circuits. International Journal of Electronics, 2000, 87, 1193-1208.	0.9	3

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91	Exploring well configurations for voltage level converter design in 28 nm UTBB FDSOI technology. , 2015, , .		3
92	Efficient Architecture for Integral Image Computation on Heterogeneous FPGAs. , 2019, , .		3
93	Automatic Microstructural Classification with Convolutional Neural Network. Advances in Intelligent Systems and Computing, 2019, , 170-181.	0.5	3
94	VLSI Implementation of a Low-Power High-Speed Self-Timed Adder. Lecture Notes in Computer Science, 2000, , 195-204.	1.0	3
95	CMOS buffer sizing for long on-chip interconnects. Electronics Letters, 1998, 34, 1937.	0.5	3
96	Tradeoffs in Digital Binary Adder Design: the effects of floorplanning, number of levels of metals, and supply voltage on performance and area. Network Theory and Applications, 2001, , 261-288.	0.6	3
97	Hybrid carry-select statistical carry look-ahead adder. Electronics Letters, 1999, 35, 549.	0.5	2
98	Design of 3:1 multiplexer standard cell. Electronics Letters, 2000, 36, 1994.	0.5	2
99	Speed-efficient wide adders for VIRTEX FPGAs. , 0, , .		2
100	FPGA implementation of Bayesian neural networks for a stand-alone predictor of pollutants concentration in the air. , 0, , .		2
101	Efficient recursive multiply architecture for FPGAs. Electronics Letters, 2005, 41, 1314.	0.5	2
102	Low-cost fully reconfigurable data-path for FPGA-based multimedia processor. , 0, , .		2
103	Tapered-V<inf>TH</inf> CMOS buffer design for improved energy efficiency in deep nanometer technology. , 2011, , .		2
104	A layout strategy for low-power voltage level shifters in 28nm UTBB FDSOI technology. , 2015, , .		2
105	Connected Component Analysis for Traffic Sign Recognition Embedded Processing Systems. , 2018, , .		2
106	A New Dynamic Logic Circuit Design for an Effective Trade-Off between Noise-Immunity, Performance and Energy Dissipation. Lecture Notes in Computer Science, 2009, , 277-286.	1.0	2
107	Hardware-Oriented Multi-Exposure Fusion Approach for Real-Time Video Processing on FPGA. , 2022, , .		2
108	High performance square rooting circuit using hybrid radix-2 adders. Electronics Letters, 1999, 35, 185.	0.5	1

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109	Designing high speed asynchronous pipelines. , 0, , .		1
110	SIMD MULTIPLIERS FOR ACCELERATING EMBEDDED PROCESSORS IN FPGAs. Journal of Circuits, Systems and Computers, 2006, 15, 537-550.	1.0	1
111	Parallel Multipliers using 3-Bit-Scan without Overlapping Bits. , 2007, , .		1
112	Power/throughput/area efficient PIM-based reconfigurable array for parallel processing. , 2008, , .		1
113	Power supply noise in accurate delay model for the sub-threshold domain. The Integration VLSI Journal, 2015, 50, 127-136.	1.3	1
114	Energy Efficient Coarse-Grain Reconfigurable Array for Accelerating Digital Signal Processing. Lecture Notes in Computer Science, 2009, , 297-306.	1.0	1
115	Heterogeneous FPGA-based System for Real-Time Drowsiness Detection. , 2022, , .		1
116	Estimation of power dissipation for transmission lines in deep-submicrometer ULSI circuits. Microwave and Optical Technology Letters, 1999, 22, 97-101.	0.9	0
117	An efficient self-timed adder realized using conventional CMOS standard cells. International Journal of Electronics, 2003, 90, 413-422.	0.9	0
118	EFFICIENT RECONFIGURABLE MANCHESTER ADDERS FOR LOW-POWER MEDIA PROCESSING. Journal of Circuits, Systems and Computers, 2005, 14, 57-63.	1.0	0
119	Impact of oxide thickness on performances of logic circuits: a predictive simulation study. , 0, , .		0
120	Design and Implementation of a 90nm Low bit-rate Image Compression Core. , 2007, , .		0
121	Quad-Port Memory Blocks in Radiation-Tolerant FPGAs: An Application for Image Processing Systems. , 2009, , .		0
122	Impact of Random Process Variations on Different 65nm SRAM Cell Topologies. , 2010, , .		0
123	VLSI Circuits for Accurate Motion Estimation. , 2010, , .		0
124	VLSI design of low-leakage single-ended 6T SRAM cell. , 2011, , .		0
125	Self-repairing SRAM architecture to mitigate the inter-die process variations at 65nm technology. Proceedings of SPIE, 2011, , .	0.8	0
126	Fastâ€squarer circuits using 3â€bitâ€scan without overlapping bits. International Journal of Circuit Theory and Applications, 2011, 39, 1037-1047.	1.3	0

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127	Optimization and evaluation of tapered-V<inf>TH</inf> approach for energy-efficient CMOS buffers. , 2011, , .		0
128	A low-cost PSoC architecture for long FFT. Proceedings of SPIE, 2013, , .	0.8	0
129	Fast Low-Power 64-Bit Modular Hybrid Adder. Lecture Notes in Computer Science, 2005, , 609-617.	1.0	0
130	A High-Performance and Power-Efficient SIMD Convolution Engine for FPGAs. , 2020, , .		0