Liang Qi

List of Publications by Year
in descending order

23 papers	162 citations	1307594 7 h-index	1199594 12 g-index
23 all docs	23 docs citations	23 times ranked	79 citing authors

#	ARTICLE	IF	CITATIONS
1	Low-Noise, High-Linearity Sine-Wave Generation Using Noise-Shaping Phase-Switching Technique. IEEE Transactions on Instrumentation and Measurement, 2022, 71, 1-7.	4.7	5
2	Background Timing Mismatch Calibration Techniques in High-Speed Time-Interleaved ADCs: A Tutorial Review. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2564-2569.	3.0	0
3	A Hybrid 1st/2nd-Order VCO-Based CTDSM With Rail-to-Rail Artifact Tolerance for Bidirectional Neural Interface. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2682-2686.	3.0	7
4	Wideband Continuous-Time MASH Delta-Sigma Modulators: A Tutorial Review. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2623-2628.	3.0	7
5	A 124 dB dynamic range sigma-delta modulator applied to non-invasive EEG acquisition using chopper-modulated input-scaling-down technique. Science China Information Sciences, 2022, 65, 1.	4.3	10
6	A VCO-Based CTDSM With Integrated Phase Error Correction for Neural Interface. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 4018-4022.	3.0	4
7	An Ultra-Low-Voltage Level Shifter With Embedded Re-Configurable Logic and Time-Borrowing Latch Technique. IEEE Access, 2021, 9, 79904-79910.	4.2	4
8	Discrete-Time MASH Delta-Sigma Modulator with Second-Order Digital Noise Coupling for Wideband High-Resolution Applications. , 2021, , .		7
9	A Multi-Rate Hybrid DT/CT Mash Î"Î£ Modulator with High Tolerance to Noise Leakage. , 2021, , .		5
10	A power-efficient and re-configurable analog artificial neural network classifier. Microelectronics Journal, 2021, 111, 105022.	2.0	5
11	A 1-Î¼A-Quiescent-Current Capacitor-Less LDO Regulator with Adaptive Embedded Slew-Rate Enhancement Circuit. , 2021, , .		2
12	An Energy-Efficient Level Shifter Using Time Borrowing Technique for Ultra Wide Voltage Conversion from Sub-200mV to 3.0V. , 2021, , .		4
13	A Time-Interleaved 2nd-Order Î"Î£ Modulator Achieving 5-MHz Bandwidth and 86.1-dB SNDR Using Digital Feed-Forward Extrapolation. IEEE Journal of Solid-State Circuits, 2021, 56, 2375-2387.	5.4	9
14	Recent Advances in High-Resolution Hybrid Discrete-Time Noise-Shaping ADCs. IEEE Open Journal of the Solid-State Circuits Society, 2021, 1, 129-139.	2.7	4
15	Self-coupled MASH Delta-Sigma Modulator with Zero Optimization. , 2021, , .		0
16	Continuous-time Delta-Sigma Modulators: Single-loop versus MASH. , 2021, , .		1
17	Advances in Continuous-time MASH Î"Î£ Modulators. , 2021, , .		0
18	Discrete-Time MASH Delta-Sigma Modulator with an IIR-based Self-Coupling. , 2021, , .		1

#	Article	IF	Citations
19	A 76.6-dB-SNDR 50-MHz-BW 29.2-mW Multi-Bit CT Sturdy MASH With DAC Non-Linearity Tolerance. IEEE Journal of Solid-State Circuits, 2020, 55, 344-355.	5.4	38
20	A Generic Nano-Watt Power Fully Tunable 1-D Gaussian Kernel Circuit for Artificial Neural Network. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1529-1533.	3.0	9
21	A Self-coupled DT MASH Î"Î£ Modulator with High Tolerance to Noise Leakage. , 2020, , .		1
22	Multibit Sturdy MASH Î"Î£ Modulator with Error-shaped Segmented DACs for Wideband Low-power Applications. , 2019, , .		0
23	A 4.2-mW 77.1-dB SNDR 5-MHz BW DT 2-1 MASH $Delta Sigma $ Modulator With Multirate Opamp Sharing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2641-2654.	5.4	39