Bingrui Wang

List of Publications by Year
in descending order

41 papers	812 citations	687363 13 h-index	642732 23 g-index
41 all docs	41 docs citations	41 times ranked	616 citing authors

#	Article	IF	Citations
1	Cambricon-S: Addressing Irregularity in Sparse Neural Networks through A Cooperative Software/Hardware Approach. , 2018, , .		136
2	MALOC: A Fully Pipelined FPGA Accelerator for Convolutional Neural Networks With All Layers Mapped on Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2601-2612.	2.7	82
3	WGAN-Based Synthetic Minority Over-Sampling Technique: Improving Semantic Fine-Grained Classification for Lung Nodules in CT Images. IEEE Access, 2019, 7, 18450-18463.	4.2	73
4	Accelerating the Next Generation Long Read Mapping with the FPGA-Based System. IEEE/ACM Transactions on Computational Biology and Bioinformatics, 2014, 11, 840-852.	3.0	43
5	Service-Oriented Architecture on FPGA-Based MPSoC. IEEE Transactions on Parallel and Distributed Systems, 2017, 28, 2993-3006.	5.6	39
6	KDnet-RUL: A Knowledge Distillation Framework to Compress Deep Neural Networks for Machine Remaining Useful Life Prediction. IEEE Transactions on Industrial Electronics, 2022, 69, 2022-2032.	7.9	36
7	Heterogeneous Cloud Framework for Big Data Genome Sequencing. IEEE/ACM Transactions on Computational Biology and Bioinformatics, 2015, 12, 166-178.	3.0	33
8	A Ubiquitous Machine Learning Accelerator With Automatic Parallelization on FPGA. IEEE Transactions on Parallel and Distributed Systems, 2020, 31, 2346-2359.	5.6	28
9	MP-Tomasulo. Transactions on Architecture and Code Optimization, 2013, 10, 1-26.	2.0	25
10	WinoNN: Optimizing FPGA-Based Convolutional Neural Network Accelerators Using Sparse Winograd Algorithm. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4290-4302.	2.7	24
11	Architecture Support for Task Out-of-Order Execution in MPSoCs. IEEE Transactions on Computers, 2015, 64, 1296-1310.	3.4	23
12	SODA: Software Defined FPGA based Accelerators for Big Data. , 2015, , .		23
13	Performance Evaluation and Optimization of HBM-Enabled GPU for Data-Intensive Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 831-840.	3.1	21
14	An Overview of FPGA Based Deep Learning Accelerators: Challenges and Opportunities. , 2019, , .		21
15	A star network approach in heterogeneous multiprocessors system on chip. Journal of Supercomputing, 2012, 62, 1404-1424.	3.6	18
16	Regarding Processors and Reconfigurable IP Cores as Services. , 2012, , .		18
17	Hardware Implementation on FPGA for Task-Level Parallel Dataflow Execution Engine. IEEE Transactions on Parallel and Distributed Systems, 2016, 27, 2303-2315.	5.6	16
18	A Flexible High Speed Star Network Based on Peer to Peer Links on FPGA. , 2011, , .		15

#	Article	IF	Citations
19	FPM: A Flexible Programming Model for MPSoC on FPGA. , 2012, , .		13
20	A power-efficient and high performance FPGA accelerator for convolutional neural networks. , 2017, , .		13
21	RV-CNN: Flexible and Efficient Instruction Set for CNNs Based on RISC-V Processors. Lecture Notes in Computer Science, 2019, , 3-14.	1.3	12
22	SOLAR: Services-oriented Deep Learning Architectures. IEEE Transactions on Services Computing, 2017, , 1-1.	4.6	11
23	GRU-ES: Resource Usage Prediction of Cloud Workloads Using a Novel Hybrid Method. , 2019, , .		11
24	WooKong: A Ubiquitous Accelerator for Recommendation Algorithms with Custom Instruction Sets on FPGA. IEEE Transactions on Computers, 2020, , 1-1.	3.4	11
25	An FPGA Based Accelerator for Clustering Algorithms With Custom Instructions. IEEE Transactions on Computers, 2021, 70, 725-732.	3.4	11
26	Improving HW/SW Adaptability for Accelerating CNNs on FPGAs through A Dynamic/Static Co-Reconfiguration Approach. IEEE Transactions on Parallel and Distributed Systems, 2020, , 1-1.	5.6	11
27	FPNet: Customized Convolutional Neural Network for FPGA Platforms. , 2019, , .		10
28	SOLAR: Services-Oriented Learning Architectures. , 2016, , .		8
29	Work-in-Progress: WinoNN: Optimising FPGA-based Neural Network Accelerators using Fast Winograd Algorithm. , 2018, , .		7
30	Higher-order Transfer Learning for Pulmonary Nodule Attribute Prediction in Chest CT Images. , 2019, , .		4
31	Addressing Irregularity in Sparse Neural Networks through a Cooperative Software/Hardware Approach. IEEE Transactions on Computers, 2020, , 1-1.	3.4	3
32	Codem: software/hardware codesign for embedded multicore systems supporting hardware services. International Journal of Electronics, 2015, 102, 32-47.	1.4	2
33	Design Exploration of Multi-FPGAs for Accelerating Deep Learning. , 2019, , .		2
34	UH-JLS: A Parallel Ultra-High Throughput JPEG-LS Encoding Architecture for Lossless Image Compression. , 2021, , .		2
35	Enabling Fast and Memory-Efficient Acceleration for Pattern Matching Workloads: The Lightweight Automata Processing Engine. IEEE Transactions on Computers, 2023, 72, 1011-1025.	3.4	2
36	Kernel-User Space Separation in DRAM Memory. , 2014, , .		1

#	Article	IF	Citations
37	LKSM: Light Weight Key-Value Store for Efficient Application Services on Local Distributed Mobile Devices. IEEE Transactions on Services Computing, 2018, , 1-1.	4.6	1
38	GenSeq+: A Scalable High-Performance Accelerator for Genome Sequencing. IEEE/ACM Transactions on Computational Biology and Bioinformatics, 2021, 18, 1512-1523.	3.0	1
39	Tinker: A Middleware for Deploying Multiple NN-Based Applications on a Single Machine. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1495-1499.	2.7	1
40	Conv-inheritance: A hardware-efficient method to compress convolutional neural networks for edge applications. Neurocomputing, 2022, 487, 172-180.	5.9	1
41	FEAS: A Faster Event-driven Accelerator Supporting Inhibitory Spiking Neural Network. , 2021, , .		0