Feng Liang

List of Publications by Year
in descending order

21	167	1307594 7	1199594 12
papers	citations	h-index	g-index

21	21	21	137
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Investigation Influence of Channel Transport on Output Characteristics in Sub-100nm Heterojunction Tunnel FET. IEEE Journal of the Electron Devices Society, 2021, 9, 783-788.	2.1	1
2	An extended context-based entropy hybrid modeling for image compression. Signal Processing: Image Communication, 2021, 95, 116244.	3.2	5
3	Posit Arithmetic Hardware Implementations with The Minimum Cost Divider and SquareRoot. Electronics (Switzerland), 2020, 9, 1622.	3.1	17
4	An Extended Hybrid Image Compression Based on Soft-to-Hard Quantification. IEEE Access, 2020, 8, 95832-95842.	4.2	8
5	Improved hybrid layered image compression using deep learning and traditional codecs. Signal Processing: Image Communication, 2020, 82, 115774.	3.2	15
6	An Accurate Analytical Model for Tunnel FET Output Characteristics. IEEE Electron Device Letters, 2019, 40, 1001-1004.	3.9	6
7	Low Cost Test Pattern Generation in Scan-Based BIST Schemes. Electronics (Switzerland), 2019, 8, 314.	3.1	7
8	An Analytical Model of Gate-All-Around Heterojunction Tunneling FET. IEEE Transactions on Electron Devices, 2018, 65, 776-782.	3.0	29
9	The Design of Objects Bounding Boxes Non-Maximum Suppression and Visualization Module Based on FPGA. , 2018, , .		5
10	Design of 16-bit fixed-point CNN coprocessor based on FPGA. , 2018, , .		4
11	Hardware Implementation for an Improved Full-Pixel Search Algorithm Based on Normalized Cross Correlation Method. Electronics (Switzerland), 2018, 7, 428.	3.1	6
12	The impact of heat loss paths on the electrothermal models of self-heating effects in nanoscale tri-gate SOI MOSFETs. IEICE Electronics Express, 2018, 15, 20180905-20180905.	0.8	2
13	A 16-BIT 200KS/S Multi-channel SAR ADC in 55nm CMOS. , 2018, , .		0
14	A Precision Voltage Reference Circuit with Trimming for 16-Bit SAR ADC in 55nm CMOS Technology. , 2018, , .		5
15	A Digital Self-Calibration Technique for 16-bit SARADC. , 2018, , .		0
16	A Full-Range Analytical Current Model for Heterojunction TFET With Dual Material Gate. IEEE Transactions on Electron Devices, 2018, 65, 5213-5217.	3.0	8
17	Test Patterns of Multiple SIC Vectors: Theory and Application in BIST Schemes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 614-623.	3.1	27
18	Low-power programmable linear-phase filter designed for fully balanced bio-signal recording application. IEICE Electronics Express, 2012, 9, 1402-1407.	0.8	5

#	Article	IF	Citations
19	A novel single event upset hardened CMOS SRAM cell. IEICE Electronics Express, 2012, 9, 140-145.	0.8	14
20	A test pattern generation method with high compression ratio. IEICE Electronics Express, 2011, 8, 1842-1847.	0.8	2
21	A Low Power Test Pattern Generator for BIST. IEICE Transactions on Electronics, 2010, E93-C, 696-702.	0.6	1