Javier Valls

List of Publications by Year in descending order

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79	1,333	516710	395702
papers	citations	16 h-index	33 g-index

80	80	80	912
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Linear Response Modeling of High Luminous Flux Phosphor-Coated White LEDs for VLC. Journal of Lightwave Technology, 2022, 40, 3761-3767.	4.6	6
2	On the Performance and Power Consumption of Bias-T Based Drivers for High Speed VLC. Journal of Lightwave Technology, 2022, 40, 6078-6086.	4.6	3
3	Syndrome-Based Min-Sum vs OSD-0 Decoders: FPGA Implementation and Analysis for Quantum LDPC Codes. IEEE Access, 2021, 9, 138734-138743.	4.2	8
4	A Computational Efficient Nyquist Shaping Approach for Short-Reach Optical Communications. Journal of Lightwave Technology, 2020, 38, 1651-1658.	4.6	1
5	A Test Vector Generation Method Based on Symbol Error Probabilities for Low-Complexity Chase Soft-Decision Reedâ€“Solomon Decoding. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2198-2207.	5.4	5
6	Second Minimum Approximation for Min-Sum Decoders Suitable for High-Rate LDPC Codes. Circuits, Systems, and Signal Processing, 2019, 38, 5068-5080.	2.0	12
7	FPGA implementation of a 10ÂGS/s variable-length FFT for OFDM-based optical communication systems. Microprocessors and Microsystems, 2019, 64, 195-204.	2.8	15
8	Soft-Decision Low-Complexity Chase Decoders for the RS(255,239) Code. Electronics (Switzerland), 2019, 8, 10.	3.1	5
9	Reedâ€“Solomon Decoder Based on a Modified ePIBMA for Low-Latency 100 Gbps Communication Systems. Circuits, Systems, and Signal Processing, 2019, 38, 1793-1810.	2.0	2
10	Real-time 2037 Gb/s optical OFDM receiver for PON IM/DD systems. Optics Express, 2018, 26, 18817.	3.4	20
11	A Fast and Low-Complexity Operator for the Computation of the Arctangent of a Complex Number. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2663-2667.	3.1	10
12	Fast- and Low-Complexity atan2(a,b) Approximation [Tips and Tricks]. IEEE Signal Processing Magazine, 2017, 34, 164-169.	5.6	9
13	Optimised CORDICâ€based atan2 computation for FPGA implementations. Electronics Letters, 2017, 53, 1296-1298.	1.0	6
14	Reduced-Complexity Nonbinary LDPC Decoder for High-Order Galois Fields Based on Trellis Minâ€“Max Algorithm. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2643-2653.	3.1	28
15	Low-Complexity Time Synchronization Algorithm for Optical OFDM PON System Using a Directly Modulated DFB Laser. Journal of Optical Communications and Networking, 2015, 7, 1025.	4.8	12
16	One Minimum Only Trellis Decoder for Non-Binary Low-Density Parity-Check Codes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 177-184.	5.4	28
17	Reduction of Complexity for Nonbinary LDPC Decoders With Compressed Messages. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2676-2679.	3.1	16
18	Simplified Trellis Minâ€“Max Decoder Architecture for Nonbinary Low-Density Parity-Check Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1783-1792.	3.1	38

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19	Efficient FPGA Hardware Reuse in a Multiplierless Decimation Chain. International Journal of Reconfigurable Computing, 2014, 2014, 1-5.	0.2	1
20	Reliability-Based Iterative Decoding Algorithm for LDPC Codes With Low Variable-Node Degree. IEEE Communications Letters, 2014, 18, 2065-2068.	4.1	1
21	Reduced-Complexity Min-Sum Algorithm for Decoding LDPC Codes With Low Error-Floor. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2150-2158.	5.4	53
22	Non-Binary LDPC Decoder Based on Symbol Flipping with Multiple Votes. IEEE Communications Letters, 2014, 18, 749-752.	4.1	29
23	Multiple-Vote Symbol-Flipping Decoder for Nonbinary LDPC Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2256-2267.	3.1	12
24	Nonbinary LDPC Decoder Based on Simplified Enhanced Generalized Bit-Flipping Algorithm. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1455-1459.	3.1	4
25	A symbol flipping decoder for NB-LDPC relying on multiple votes. , 2014, , .		0
26	High-speed NB-LDPC decoder for wireless applications. , 2013, , .		4
27	Architecture of Generalized Bit-Flipping Decoding for High-Rate Non-binary LDPC Codes. Circuits, Systems, and Signal Processing, 2013, 32, 727-741.	2.0	7
28	Low latency T-EMS decoder for non-binary LDPC codes. , 2013, , .		15
29	Serial Symbol-Reliability Based Algorithm for Decoding Non-Binary LDPC Codes. IEEE Communications Letters, 2012, 16, 909-912.	4.1	9
30	High-Throughput Interpolator Architecture for Low-Complexity Chase Decoding of RS Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 568-573.	3.1	6
31	Decoder for an enhanced serial generalized bit flipping algorithm. , 2012, , .		4
32	Fully-parallel LUT-based (2048,1723) LDPC code decoder for FPGA. , 2012, , .		4
33	High-throughput FPGA-based emulator for structured LDPC codes. , 2012, , .		6
34	Hardware Architecture of a Gaussian Noise Generator Based on the Inversion Method. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 501-505.	3.0	16
35	Modified Shuffled Based Architecture for High-Throughput Decoding of LDPC Codes. Journal of Signal Processing Systems, 2012, 68, 139-149.	2.1	0
36	Low Complexity Time Synchronization Algorithm for OFDM Systems with Repetitive Preambles. Journal of Signal Processing Systems, 2012, 68, 287-301.	2.1	5

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37	FPGA implementation of an OFDM-based WLAN receiver. Microprocessors and Microsystems, 2012, 36, 232-244.	2.8	17
38	Improved Sliced Message Passing Architecture for High Throughput Decoding of LDPC Codes. Journal of Signal Processing Systems, 2012, 66, 99-104.	2.1	2
39	Low Cost Hardware Implementation of Logarithm Approximation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 2326-2330.	3.1	53
40	High-Speed RS(255, 239) Decoder Based on LCC Decoding. Circuits, Systems, and Signal Processing, 2011, 30, 1643-1669.	2.0	25
41	FPGA-implementation of atan(Y/X) based on logarithmic transformation and LUT-based techniques. Journal of Systems Architecture, 2010, 56, 588-596.	4.3	17
42	POWER CONSUMPTION REDUCTION IN A VITERBI DECODER FOR OFDM-WLAN. Journal of Circuits, Systems and Computers, 2009, 18, 1333-1337.	1.5	0
43	Design and FPGA-Implementation of a High Performance Timing Recovery Loop for Broadband Communications. Journal of Signal Processing Systems, 2009, 56, 17-23.	2.1	1
44	Low-Power FPGA-Implementation of atan(Y/X) Using Look-Up Table Methods for Communication Applications. Journal of Signal Processing Systems, 2009, 56, 25-33.	2.1	10
45	Design of Power and Area Efficient Digital Down-converters for Broadband Communications Systems. Journal of Signal Processing Systems, 2009, 56, 35-40.	2.1	3
46	FPGA-implementation of Time-Multiplexed Multiple Constant Multiplication based on carry-save arithmetic. , 2009, , .		3
47	50 Years of CORDIC: Algorithms, Architectures, and Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1893-1907.	5.4	424
48	Architectures for the Implementation of a OFDM-WLAN Viterbi Decoder. Journal of Signal Processing Systems, 2008, 52, 35-44.	2.1	5
49	Efficient Mapping of CORDIC Algorithm for OFDM-Based WLAN. Journal of Signal Processing Systems, 2008, 52, 181-191.	2.1	12
50	64-QAM 4×4 MIMO decoders based on Successive Projection Algorithm. , 2008, , .		2
51	Time Synchronization for the IEEE 802.11a/g WLAN Standard. , 2007, , .		4
52	Implementation on FPGA of a LUT-Based atan(Y/X) Operator Suitable for Synchronization Algorithms. , 2007, , .		10
53	Reduction of power consumption in a Viterbi Decoder for OFDM-WLAN. , 2007, , .		0
54	Design of an efficient digital down-converter for a SDR-based DVB-S receiver. , 2007, , .		0

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55	FFT Spectrum Analyzer Project for Teaching Digital Signal Processing With FPGA Devices. IEEE Transactions on Education, 2007, 50, 229-235.	2.4	32
56	Scheme for Reducing the Storage Requirements of FFT Twiddle Factors on FPGAs. Journal of Signal Processing Systems, 2007, 47, 183-187.	1.0	7
57	Design of high performance timing recovery loops for communication applications. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2006, , .	0.0	2
58	The use of CORDIC in software defined radios: a tutorial. , 2006, 44, 46-50.		65
59	Efficient pipeline FFT processors for WLAN MIMO-OFDM systems. Electronics Letters, 2005, 41, 1043.	1.0	38
60	Hardware Design of a FPGA-Based Synchronizer for Hiperlan/2. Lecture Notes in Computer Science, 2004, , 494-504.	1.3	1
61	Digit-Serial Complex-Number Multipliers on FPGAs. Journal of Signal Processing Systems, 2003, 33, 105-115.	1.0	3
62	Efficient fpga-implementation of two's complement digit-serial/parallel multipliers. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2003, 50, 317-322.	2.2	6
63	Area-efficient FPGA-based FFT processor. Electronics Letters, 2003, 39, 1369.	1.0	20
64	DIGIMOD: A Tool to Implement FPGA-Based Digital IF and Baseband Modems. Lecture Notes in Computer Science, 2003, , 988-991.	1.3	0
65	Evaluation of CORDIC Algorithms for FPGA Design. Journal of Signal Processing Systems, 2002, 32, 207-222.	1.0	60
66	A study about FPGA-based digital filters. , 0, , .		11
67	Design and FPGA implementation of digit-serial FIR filters. , 0, , .		9
68	Fast FPGA-based pipelined digit-serial/parallel multipliers. , 0, , .		10
69	Digit-serial fixed coefficient complex number multiplier-accumulator on FPGAs. , 0, , .		2
70	FPGA-based digit-serial complex number multiplier-accumulator. , 0, , .		2
71	Distributed arithmetic radix-2 butterflies for FPGA. , 0, , .		2
72	FPGA based on-line complex-number multipliers. , 0, , .		1

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73	FPGA-based radix-4 butterflies for HIPERLAN/2. , 0, , .		7
74	Design of a digital front-end transmitter for ofdm-wlan systems using fpga. , 0, , .		10
75	FPGA implementation of an if transceiver for OFDM-based WLAN. , 0, , .		16
76	A common FPGA based synchronizer architecture for Hiperlan/2 and IEEE 802.11a WLAN systems. , 0, , .		4
77	Efficient mapping on FPGA of a viterbi decoder for wireless LANs. , 0, , .		3
78	Statistical power estimation for FPGAs. , 0, , .		10
79	Efficient fpga implementation of cordic algorithm for circular and linear coordinates. , 0, , .		23