Chih-Chi Cheng

List of Publications by Year
in descending order

24	218	1478505 6	1588992 8
papers	citations	h-index	g-index

25	25	25	157
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Multimode Embedded Compression Codec Engine for Power-Aware Video Coding System. IEEE Transactions on Circuits and Systems for Video Technology, 2009, 19, 141-150.	8.3	54
2	iVisual: An Intelligent Visual Sensor SoC With 2790 fps CMOS Image Sensor and 205 GOPS/W Vision Processor. IEEE Journal of Solid-State Circuits, 2009, 44, 127-135.	5.4	37
3	On-Chip Memory Optimization Scheme for VLSI Implementation of Line-Based Two-Dimentional Discrete Wavelet Transform. IEEE Transactions on Circuits and Systems for Video Technology, 2007, 17, 814-822.	8.3	20
4	iVisual: An Intelligent Visual Sensor SoC with 2790fps CMOS Image Sensor and 205GOPS/W Vision Processor. , 2008, , .		15
5	Multi-mode embedded compression codec engine for power-aware video coding system. , 0, , .		13
6	Precompression Quality-Control Algorithm for JPEG 2000. IEEE Transactions on Image Processing, 2006, 15, 3279-3293.	9.8	11
7	Efficient Architecture Design of Motion-Compensated Temporal Filtering/Motion Compensated Prediction Engine. IEEE Transactions on Circuits and Systems for Video Technology, 2008, 18, 98-109.	8.3	8
8	Memory Efficient JPEG 2000 Architecture with Stripe Pipeline Scheme. , 0, , .		7
9	A 5mW MPEG4 SP encoder with 2D bandwidth-sharing motion estimation for mobile applications. , 2006, , .		7
10	Multiple-lifting Scheme: Memory-efficient VLSI Implementation for Line-based 2-D DWT. , 0, , .		6
11	Memory Efficient JPEG 2000 Architecture With Stripe Pipeline Scheduling. IEEE Transactions on Signal Processing, 2006, 54, 4807-4816.	5.3	6
12	124 MSamples/s Pixel-Pipelined Motion-JPEG 2000 Codec Without Tile Memory. IEEE Transactions on Circuits and Systems for Video Technology, 2007, 17, 398-406.	8.3	6
13	A 216fps 4096×2160p 3DTV set-top box SoC for free-viewpoint 3DTV applications. , 2011, , .		5
14	Quad Full-HD Transform Engine for Dual-Standard Low-Power Video Coding. IEEE Journal of Solid-State Circuits, 2012, 47, 2724-2736.	5.4	5
15	Line Buffer Wordlength Analysis for Line-Based 2-D DWT. , 0, , .		4
16	124Ms/s pixel-pipelined motion-JPEG 2000 codec without tile memory. , 2006, , .		4
17	Quad Full-HD transform engine for dual-standard low-power video coding. , 2011, , .		4
18	System Architecture Design Methodology for H.264/AVC Encoder. , 2007, , .		3

#	Article	IF	Citations
19	Frame-level data reuse for motion-compensated temporal filtering. , 0, , .		2
20	Application Layer Error Correction Scheme for Video Header Protection on Wireless Network. , 0, , .		1
21	Scalable Rate-Distortion-Computation Hardware Accelerator for MCTF and ME. , 2006, , .		0
22	Analysis and VLSI architecture of update step in motion-compensated temporal filtering. , 0, , .		0
23	Diastolic arrays: Throughput-driven reconfigurable computing. , 2008, , .		0
24	A 0.077 to 0.168 nJ/bit/iteration scalable 3GPP LTE turbo decoder with an adaptive sub-block parallel scheme and an embedded DVFS engine. , 2010, , .		0