B Bindu

List of Publications by Year
in descending order

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41	243	1163117	1125743
papers	citations	8 h-index	13 g-index

41	41	41	176
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A push-pulled capacitor-less FVF LDO with active feed-forward compensator. International Journal of Electronics, 2021, 108, 684-704.	1.4	6
2	A transient enhanced cap-less low-dropout regulator for wide range of load currents and capacitances. Microelectronics Journal, 2021, 115, 105207.	2.0	7
3	Sensitivity of SET Pulse-Width and Propagation to Radiation Track Parameters in CMOS Inverter Chain. IETE Journal of Research, 2020, , 1-9.	2.6	1
4	A Physics-Based Single Event Transient Pulse Width Model for CMOS VLSI Circuits. IEEE Transactions on Device and Materials Reliability, 2020, 20, 723-730.	2.0	9
5	A Cap-less Voltage Spike Detection and Correction Circuit for Low Dropout Regulator. Journal of Circuits, Systems and Computers, 2020, 29, 2020009.	1.5	2
6	High-PSR Capacitorless LDO with Adaptive Circuit for Varying Loads. Journal of Circuits, Systems and Computers, 2020, 29, 2050178.	1.5	7
7	A physics-based model for LER-induced threshold voltage variations in double-gate MOSFET. Journal of Computational Electronics, 2020, 19, 622-630.	2.5	5
8	Dual-summed flipped voltage follower LDO regulator with active feed-forward compensation. AEU - International Journal of Electronics and Communications, 2020, 123, 153314.	2.9	20
9	Capacitorâ€less FVF low dropâ€out regulator with active feedâ€forward compensation and efficient slewâ€rate enhancer circuit. IET Circuits, Devices and Systems, 2020, 14, 853-859.	1.4	6
10	An Analytical Model of Single-Event Transients in Double-Gate MOSFET for Circuit Simulation. IEEE Transactions on Electron Devices, 2019, 66, 3710-3717.	3.0	14
11	Analytical modeling of random discrete traps induced threshold voltage fluctuations in double-gate MOSFET with HfO2/SiO2 gate dielectric stack. Microelectronics Reliability, 2019, 99, 87-95.	1.7	2
12	Analytical Model for RDF-Induced Threshold Voltage Fluctuations in Double-Gate MOSFET. IEEE Transactions on Device and Materials Reliability, 2019, 19, 370-377.	2.0	3
13	Analysis of bipolar amplification due to heavy-ion irradiation in 45â€¯nm FDSOI MOSFET with thin BOX and ground plane. Microelectronics Reliability, 2019, 98, 56-62.	1.7	5
14	Design and Optimization of Double-Gate MOSFET to Reduce the Effects of Single Event Transients. Springer Proceedings in Physics, 2019, , 583-588.	0.2	1
15	A physics-based 3-D potential and threshold voltage model for undoped triple-gate FinFET with interface trapped charges. Journal of Computational Electronics, 2019, 18, 37-45.	2.5	8
16	Analytical model of hot carrier degradation in uniaxial strained triple-gate FinFET for circuit simulation. Journal of Computational Electronics, 2018, 17, 163-171.	2.5	7
17	Hot Carrier Reliability in 45 nm Strained Si/relaxed Si_{1â^'x}Ge_x CMOS Based SRAM Cell. , 2018, , .		1
18	A Review on Circuit Simulation Techniques of Single-Event Transients and their Propagation in Delay Locked Loop. IETE Technical Review (Institution of Electronics and Telecommunication Engineers,) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50	3.2	12

#	Article	IF	Citations
19	A capacitor-less low-dropout regulator (LDO) architecture for wireless application. , 2017, , .		0
20	Impact of NBTI induced variations on FinFET based Vernier delay line time to digital converter. , 2017, , .		0
21	Widening and narrowing of time interval due to singleâ€event transients in 45â€…nm vernierâ€type TDC. IET Circuits, Devices and Systems, 2017, 11, 676-681.	1.4	4
22	A physics based analytical model and numerical simulation for current-voltage characteristics of microwave power AlGaN/GaN HEMT. , 2016, , .		1
23	Impact of NBTI induced variations on delay locked loop multi-phase clock generator. Microelectronics Reliability, 2016, 60, 33-40.	1.7	8
24	Modification of electrical properties of Au/n-type InP Schottky diode with a high-k Ba 0.6 Sr 0.4 TiO 3 interlayer. Superlattices and Microstructures, 2016, 93, 82-91.	3.1	31
25	A Physics-Based Model of Double-Gate Tunnel FET for Circuit Simulation. IETE Journal of Research, 2016, 62, 387-393.	2.6	8
26	Design of FinFET based frequency synthesizer. , 2015, , .		0
27	Design of FinFET based All-Digital DLL for multiphase clock generation. , 2015, , .		2
28	Low power, high speed carbon nanotube FET based level shifters for multi-VDD Systems-On-Chips. Microelectronics Journal, 2015, 46, 1269-1274.	2.0	8
29	Design of tunnel FET based low power digital circuits. , 2014, , .		2
30	Reliability studies of AlGaN/GaN high electron mobility transistors (HEMT). , 2012, , .		0
31	Random Dopant induced variability in SOI trigate FINFET: A simulation study. , 2012, , .		0
32	Feasibility Study of Conical Channel Nanowire MOSFETs for Improved Performance. Procedia Engineering, 2012, 38, 2364-2370.	1.2	2
33	Simulation studies of Negative Bias Temperature Instability in FinFETs using two-stage model. , 2012, , .		0
34	Parameter set and data sampling strategy for accurate yet efficient statistical MOSFET compact model extraction. Solid-State Electronics, 2010, 54, 307-315.	1.4	10
35	Analytical solution of the switching trap model for negative bias temperature stress. , 2009, , .		11
36	A Unified Model for Gate Capacitanceâ€“Voltage Characteristics and Extraction of Parameters of Si/SiGe Heterostructure pMOSFETs. IEEE Transactions on Electron Devices, 2007, 54, 1889-1896.	3.0	12

#	Article	IF	Citations
37	Analytical model of drain current of strained-Si/strained-Si1â^'YGeY/relaxed-Si1â^'XGeX NMOSFETs and PMOSFETs for circuit simulation. Solid-State Electronics, 2006, 50, 448-455.	1.4	11
38	Design of single-gate n-channel and p-channel MOSFETs with enhanced current-drive due to simultaneous switching of front and back channels in SOI CMOS technology. Solid-State Electronics, 2006, 50, 1359-1367.	1.4	2
39	Analytical model of drain current of Si/SiGe heterostructure p-channel MOSFETs for circuit simulation. IEEE Transactions on Electron Devices, 2006, 53, 1411-1419.	3.0	15
40	Virtual Double-Gate Operation in Conventional SOI CMOS Technology. , 0, , .		0
41	A Low Power Voltage Spike Detection Circuit for Cap-less LDO. International Journal of Electronics Letters, 0, , 1-14.	1.2	0