Dionysios Reisis

List of Publications by Year
in descending order

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58	317	1040056	1058476
papers	citations	9	14
		h-index	g-index

58	58	58	301
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Conflict-Free Parallel Memory Accessing Techniques for FFT Architectures. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 3438-3447.	5.4	33
2	Reduced Complexity Superresolution for Low-Bitrate Video Compression. IEEE Transactions on Circuits and Systems for Video Technology, 2016, 26, 332-345.	8.3	25
3	Acceleration techniques and evaluation on multi-core CPU, GPU and FPGA for image processing and super-resolution. Journal of Real-Time Image Processing, 2019, 16, 1207-1234.	3.5	23
4	A real-time motion estimation FPGA architecture. Journal of Real-Time Image Processing, 2008, 3, 3-20.	3.5	20
5	An efficient dual-mode floating-point Multiply-Add Fused Unit. , 2010, , .		17
6	High Performance Accelerator for CNN Applications. , 2019, , .		14
7	An efficient multiple precision floating-point multiplier. , 2011, , .		13
8	An efficient multiple precision floating-point Multiply-Add Fused unit. Microelectronics Journal, 2016, 49, 10-18.	2.0	13
9	A real-time H.264/AVC VLSI encoder architecture. Journal of Real-Time Image Processing, 2008, 3, 43-59.	3.5	11
10	LDPC Hardware Acceleration in 5G Open Radio Access Network Platforms. IEEE Access, 2021, 9, 152960-152971.	4.2	11
11	Fully Systolic FFT Architecture for Giga-sample Applications. Journal of Signal Processing Systems, 2010, 58, 281-299.	2.1	10
12	Design and Comparison of FFT VLSI Architectures for SoC Telecom Applications with Different Flexibility, Speed and Complexity Trade-Offs. Circuits, Systems, and Signal Processing, 2012, 31, 627-649.	2.0	9
13	Address Generation Techniques for Conflict Free Parallel Memory Accessing in FFT Architectures. , 2006, , .		8
14	Exact Max-Log MAP Soft-Output Sphere Decoding via Approximate Schnorrâ€“Euchner Enumeration. IEEE Transactions on Vehicular Technology, 2015, 64, 2749-2753.	6.3	8
15	A novel architecture for efficient protocol processing in high speed communication environments. , 0, , .		7
16	Slotted TDMA and optically switched network for disaggregated datacenters. , 2017, , .		7
17	An Efficient H.264 VLSI Advanced Video Encoder. , 2006, , .		6
18	A High Performance VLSI FFT Architecture. , 2006, , .		5

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19	Addressing technique for parallel memory accessing in radix-2 FFT processors. , 2008, , .		5
20	Study of interpolation filters for motion estimation with application in H.264/AVC encoders. , 2011, , .		5
21	Resources and Power Efficient FPGA Accelerators for Real-Time Image Classification. Journal of Imaging, 2022, 8, 114.	3.0	5
22	High Performance 16K, 64K, 256K complex points VLSI Systolic FFT Architectures. , 2007, , .		4
23	Evaluating the performance of a configurable, extensible VLIW processor in FFT execution. , 2009, , .		4
24	A continuous-flow, Variable-Length FFT SDF architecture. , 2010, , .		4
25	Single-image super-resolution using low complexity adaptive iterative back-projection. , 2013, , .		4
26	Design and Performance Comparison of CNN Accelerators Based on the Intel Movidius Myriad2 SoC and FPGA Embedded Prototype. , 2019, , .		4
27	A Parallel VLSI Video/Communication Controller. Journal of Signal Processing Systems, 2001, 28, 245-257.	1.0	3
28	Efficient Systolic Array Mapping of FIR Filters Used in PAM-QAM Modulators. Journal of Signal Processing Systems, 2003, 35, 179-186.	1.0	3
29	A VLSI architecture for minimizing the transmission power in OFDM transceivers. , 0, , .		3
30	A Control-Theoretic Approach for Efficient Design ofÂFilters in DAC and Digital Audio Amplifiers. Circuits, Systems, and Signal Processing, 2011, 30, 421-438.	2.0	3
31	Switching functions of a data center Top-of-Rack (ToR). , 2016, , .		3
32	Parallel Memory Accessing for FFT Architectures. Journal of Signal Processing Systems, 2018, 90, 1593-1607.	2.1	3
33	An efficient component (IN-RAM) for buffer management and multi-protocol implementation in ATM systems. , 0, , .		2
34	Title is missing!. Telecommunication Systems, 2003, 23, 351-367.	2.5	2
35	A Graphics Parallel Memory Organization Exploiting Request Correlations. IEEE Transactions on Computers, 2010, 59, 762-775.	3.4	2
36	Configurable baseband digital transceiver for Gbps wireless 60 GHz communications. , 2011, , .		2

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37	Conflict free, parallel memory access for radix-2 FFT processors. , 2012, , .		2
38	FPGA design of the decoding functions in the physical layer adaptation subsystem of the XG-PON optical network unit/terminal. , 2014, , .		2
39	End-to-End Real-Time Demonstration of the Slotted, SDN-Controlled NEPHELE Optical Datacenter Network. Photonics, 2020, 7, 44.	2.0	2
40	Calculation of the Power of the Reflected Radiation Modes from an Abruptly Terminated Single-Mode-Fiber Waveguide. Electromagnetics, 1995, 15, 513-526.	0.7	1
41	An efficient digital FIR filter design for 64 QAM. , 0, , .		1
42	A new FFT architecture for 4 × 4 MIMO-OFDMA systems with variable symbol lengths. , 2009, , .		1
43	Efficient cascaded VLSI FFT architecture for OFDM systems. , 2009, , .		1
44	A configurable length, Fused Multiply-Add floating point unit for a VLIW processor. , 2009, , .		1
45	Neuronal connectivity assessment for epileptic seizure prevention: Parallelizing the generalized partial directed coherence on many-core platforms. , 2014, , .		1
46	GUI for the communication agent of the â€œNepheleâ€•data center. , 2017, , .		1
47	Realizing virtual output queues in high throughput data center nodes. , 2017, , .		1
48	Parallel Robust Absolute Orientation on FPGA for Vision and Robotics. , 2018, , .		1
49	Parity Based In-Place FFT Architecture for Continuous Flow Applications. , 2018, , .		1
50	A modular VLSI architecture for real-time processing of video streaming applications over ATM network. , 0, , .		0
51	An approach for efficient design of digital amplifiers. , 0, , .		0
52	Thread-Parallel MPEG-2 and MPEG-4 Encoders for Shared-Memory System-On-Chip Multiprocessors. International Journal of Computers and Applications, 2007, 29, 353-361.	1.3	0
53	Programmable Motion Estimation architecture. , 2009, , .		0
54	Signal processing for deep-sea observatories with reconfigurable hardware. , 2012, , .		0

#	Article	IF	Citations
55	Using high-level synthesis to build memory and datapath optimized DSP accelerators. , 2014, , .		0
56	Towards real-time neuronal connectivity assessment: A scalable pipelined parallel generalized partial directed coherence engine. , 2015, , .		0
57	GUI for the communication agent of the â€œNepheleâ€•Data Center. , 2017, , .		0
58	Towards sharing one FPGA SoC for both low-level PHY and high-level AI/ML computing at the edge. , 2021, , .		0