

Nitin Chandrachoodan

List of Publications by Year in descending order

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Version: 2024-02-01

51
papers

202
citations

1937685

4
h-index

1372567

10
g-index

51
all docs

51
docs citations

51
times ranked

187
citing authors

#	ARTICLE	IF	CITATIONS
1	FPGA-Based High-Performance and Scalable Block LU Decomposition Architecture. IEEE Transactions on Computers, 2012, 61, 60-72.	3.4	51
2	GPU Implementation of a Programmable Turbo Decoder for Software Defined Radio Applications. , 2012, , .		20
3	DFT Assisted Techniques for Peak Launch-to-Capture Power Reduction during Launch-On-Shift At-Speed Testing. ACM Transactions on Design Automation of Electronic Systems, 2015, 21, 1-25.	2.6	18
4	EOG based virtual keyboard. , 2015, , .		12
5	Adaptive negative cycle detection in dynamic graphs. , 2001, , .		11
6	Implementation of a 30 ps resolution time to digital converter in FPGA. , 2015, , .		7
7	Probabilistic Error Modeling for Two-part Segmented Approximate Adders. , 2018, , .		7
8	A GPU implementation of belief propagation decoder for polar codes. , 2012, , .		6
9	Optimizing power-accuracy trade-off in approximate adders. , 2018, , .		6
10	Layout-Aware and Programmable Memory BIST Synthesis for Nanoscale System-on-Chip Designs. , 2008, , .		5
11	iitRACE: A memory efficient engine for fast incremental timing analysis and clock pessimism removal. , 2015, , .		5
12	FFT/IFFT implementation using Vivadoâ„¢ HLS. , 2016, , .		5
13	Optimization of Signal Processing Applications Using Parameterized Error Models for Approximate Adders. Transactions on Embedded Computing Systems, 2021, 20, 1-25.	2.9	5
14	An efficient timing model for hardware implementation of multirate dataflow graphs. , 2001, , .		4
15	The hierarchical timing pair model for multirate DSP applications. IEEE Transactions on Signal Processing, 2004, 52, 1209-1217.	5.3	4
16	Efficient Implementation of IEEE Double Precision Floating-Point Multiplier on FPGA. , 2008, , .		4
17	A Simulation-Based Metric to Guide Glitch Power Reduction in Digital Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 376-386.	3.1	4
18	Scalable low power digital filter architectures for varying input dynamic range. , 2013, , .		3

#	ARTICLE	IF	CITATIONS
19	EASpiNN: Effective Automated Spiking Neural Network Evaluation on FPGA. , 2020, , .		3
20	Analysis of powerâ€“accuracy tradeâ€“off in digital signal processing applications using lowâ€“power approximate adders. IET Computers and Digital Techniques, 2021, 15, 97-111.	1.2	3
21	The hierarchical timing pair model. , 2001, , .		2
22	Efficient Implementation of Floating-Point Reciprocator on FPGA. , 2009, , .		2
23	Non-uniform DFT implementation for channel simulations in GPU. , 2015, , .		2
24	Scenario-Aware Dynamic Power Reduction Using Bias Addition. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 450-461.	3.1	2
25	A scalable pseudo-exhaustive search for fault diagnosis in microfluidic biochips. , 2017, , .		2
26	Lossless Parallel Implementation of a Turbo Decoder on GPU. , 2018, , .		2
27	Speeding up computation of the max/min of a set of gaussians for statistical timing analysis and optimization. , 2013, , .		1
28	An investigation of passive optical networks for India based neutrino observatory. , 2013, , .		1
29	Designing a passive star optical network for the India-based Neutrino Observatory. , 2015, , .		1
30	White Mirror. , 2019, , .		1
31	Scalable pseudoâ€“exhaustive methodology for testing and diagnosis in flowâ€“based microfluidic biochips. IET Computers and Digital Techniques, 2020, 14, 122-131.	1.2	1
32	Probabilistic Spike Propagation for Efficient Hardware Implementation of Spiking Neural Networks. Frontiers in Neuroscience, 2021, 15, 694402.	2.8	1
33	A Smoothed LASSO-Based DNN Sparsification Technique. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4287-4298.	5.4	1
34	High-Level Synthesis of DSP Applications Using Adaptive Negative Cycle Detection. Eurasip Journal on Advances in Signal Processing, 2002, 2002, 1.	1.7	0
35	A Novel Event Based Simulation Algorithm for Sequential Digital Circuit Simulation. , 2007, , .		0
36	Rapid Abstract Control Model for Signal Processing Implementation. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2007, , .	0.0	0

#	ARTICLE	IF	CITATIONS
37	Memory Yield Improvement through Multiple Test Sequences and Application-Aware Fault Models. , 2008, , .		0
38	Post-Synthesis Circuit Techniques for Runtime Leakage Reduction. , 2011, , .		0
39	PinPoint: An algorithm for enhancing diagnostic resolution using capture cycle power information. , 2013, , .		0
40	Tutorial T1B: Riding the "Energy Consumption Horse" - from System-level Design to Silicon. , 2013, , .		0
41	An inertial sensor-based system to develop motor capacity in children with cerebral palsy. , 2013, 2013, 6111-4.		0
42	Scalable Low Power FFT/IFFT Architecture with Dynamic Bit Width Configurability. , 2014, , .		0
43	Design of flight computer module for IITMSAT. , 2015, , .		0
44	Effect of stimulation shapes on the Steady-State Visual-Evoked response. , 2015, , .		0
45	Design of command and Data Management System for IITMSAT. , 2015, , .		0
46	Guided multilevel approximation of less significant bits for power reduction. , 2016, , .		0
47	Depending on HTTP/2 for Privacy? Good Luck!. , 2020, , .		0
48	24th "IEEE International Conference on VLSI Design" Chennai, India, 2â€“7 January 2011. Journal of Low Power Electronics, 2011, 7, 459-459.	0.6	0
49	Interconnect Aware Test Power Reduction. Journal of Low Power Electronics, 2012, 8, 516-525.	0.6	0
50	Design of a Spectrometer for Frequency Domain Optical Coherence Tomography Working at 1325 nm. , 2017, , .		0
51	FPGA Implementation of Non-Uniform DFT for Accelerating Wireless Channel Simulations (Abstract) Tj ETQq1 1 0.784314 rgBT /Overl		0