Sebastien Pillement

List of Publications by Year
in descending order

39	232	1307594 7	1199594 12
papers	citations	h-index	g-index

39	39	39	171
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Energy-Efficient GPS Synchronization for Wireless Nodes. IEEE Sensors Journal, 2021, 21, 5221-5229.	4.7	10
2	A Measurement-Based Message-Level Timing Prediction Approach for Data-Dependent SDFGs on Tile-Based Heterogeneous MPSoCs. Applied Sciences (Switzerland), 2021, 11, 6649.	2.5	1
3	System-Level Modeling and Simulation of MPSoC Run-Time Management Using Execution Traces Analysis. Lecture Notes in Computer Science, 2019, , 281-293.	1.3	0
4	FTUC: A Flooding Tree Uneven Clustering Protocol for a Wireless Sensor Network. Sensors, 2017, 17, 2706.	3.8	2
5	OCEAN, a flexible adaptive Network-On-Chip for dynamic applications. Microprocessors and Microsystems, 2014, 38, 337-357.	2.8	0
6	Low-overhead fault-tolerance technique for a dynamically reconfigurable softcore processor. IEEE Transactions on Computers, 2013, 62, 1179-1192.	3.4	47
7	Cluster based MPSoC architecture: an on-chip message passing implementation. Design Automation for Embedded Systems, 2013, 17, 587-607.	1.0	2
8	Towards future adaptive multiprocessor systems-on-chip: An innovative approach for flexible architectures. , 2012, , .		10
9	Impact of design parameters on performance of adaptive Network-on-Chips. , 2012, , .		3
10	Communication service for hardware tasks executed on dynamic and partial reconfigurable resources. , 2011, , .		3
11	Error recovery technique for coarse-grained reconfigurable architectures. , 2011, , .		17
12	A framework for the design of reconfigurable fault tolerant architectures. , 2011, , .		0
13	Re²DA: Reliable and reconfigurable dynamic architecture. , 2011, , .		3
14	Real-time scheduling on heterogeneous system-on-chip architectures using an optimised artificial neural network. Journal of Systems Architecture, 2011, 57, 340-353.	4.3	8
15	Hardware OS Communication Service and Dynamic Memory Management for RSoCs. , 2011, , .		2
16	RANN: A Reconfigurable Artificial Neural Network Model for Task Scheduling onÂReconfigurable System-on-Chip. Lecture Notes in Electrical Engineering, 2011, , 117-144.	0.4	0
17	Spatio-temporal coding to improve speed and noise tolerance of on-chip interconnect. Microelectronics Journal, 2010, 41, 480-486.	2.0	0
18	Flexible Interconnection Network for Dynamically and Partially Reconfigurable Architectures. International Journal of Reconfigurable Computing, 2010, 2010, 1-15.	0.2	11

#	Article	IF	Citations
19	Design of a fault-tolerant coarse-grained. , 2010, , .		17
20	Designing Efficient Codecs for Bus-Invert Berger Code for Fully Asymmetric Communication. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 777-781.	3.0	10
21	Comments on "A Low-Power Dependable Berger Code for Fully Asymmetric Communication". IEEE Communications Letters, 2010, 14, 761-763.	4.1	0
22	Evaluation of Fault-Mitigation Schemes for Fault-Tolerant Dynamic MPSoC. , 2010, , .		2
23	Task placement for dynamic and partial reconfigurable architecture. , 2010, , .		12
24	R2NoC: Dynamically Reconfigurable Routers for Flexible Networks on Chip. , 2010, , .		2
25	OveRSoC: A Framework for the Exploration of RTOS for RSoC Platforms. International Journal of Reconfigurable Computing, 2009, 2009, 1-22.	0.2	12
26	A Fault-Tolerant Layer for Dynamically Reconfigurable Multi-processor System-on-Chip. , 2009, , .		10
27	Flexible communication support for dynamically reconfigurable FPGAS. , 2009, , .		5
28	DRAFT: Flexible interconnection network for dynamically reconfigurable architectures. , 2009, , .		2
29	xMAML: A Modeling Language for Dynamically Reconfigurable Architectures. , 2009, , .		4
30	Reconfigurable ECU communications in Autosar Environment. , 2009, , .		4
31	Efficient and Flexible Dynamic Reconfiguration for Multi Context Architectures. Journal of Integrated Circuits and Systems, 2009, 4, 36-44.	0.4	1
32	A new approach of coding to improve speed and noise tolerance of on-chip busses. , 2008, , .		3
33	Efficient dynamic reconfiguration for multi-context embedded FPGA. , 2008, , .		2
34	DART: A Functional-Level Reconfigurable Architecture for High Energy Efficiency. Eurasip Journal on Embedded Systems, 2008, 2008, 1-13.	1.2	19
35	A Neural Network Model for Real-Time Scheduling on Heterogeneous SoC Architectures. Neural Networks (IJCNN), International Joint Conference on, 2007, , .	0.0	6
36	Architectures reconfigurable et faible consommation. RÃ©alitÃ© ou prospective ?. Techniques Et Sciences Informatiques, 2007, 26, 595-621.	0.0	0

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37	Du microprocesseur au circuit FPGA. Une analyse sous l'angle de la reconfiguration. Techniques Et Sciences Informatiques, 2005, 24, 395-422.	0.0	0
38	Energy- Efficient Reconfigurable Processors. Computer Engineering Series, 2004, , 20-1-20-15.	0.1	1
39	Mapping future generation mobile telecommunication applications on a dynamically reconfigurable arcidtecture. , 2002, , .		1