

# Sebastien Pillement

## List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/6778994/publications.pdf>

Version: 2024-02-01

39  
papers

232  
citations

1307594

7  
h-index

1199594

12  
g-index

39  
all docs

39  
docs citations

39  
times ranked

171  
citing authors

#	ARTICLE	IF	CITATIONS
1	Low-overhead fault-tolerance technique for a dynamically reconfigurable softcore processor. IEEE Transactions on Computers, 2013, 62, 1179-1192.	3.4	47
2	DART: A Functional-Level Reconfigurable Architecture for High Energy Efficiency. Eurasip Journal on Embedded Systems, 2008, 2008, 1-13.	1.2	19
3	Design of a fault-tolerant coarse-grained. , 2010, , .		17
4	Error recovery technique for coarse-grained reconfigurable architectures. , 2011, , .		17
5	OverRSoc: A Framework for the Exploration of RTOS for RSoC Platforms. International Journal of Reconfigurable Computing, 2009, 2009, 1-22.	0.2	12
6	Task placement for dynamic and partial reconfigurable architecture. , 2010, , .		12
7	Flexible Interconnection Network for Dynamically and Partially Reconfigurable Architectures. International Journal of Reconfigurable Computing, 2010, 2010, 1-15.	0.2	11
8	A Fault-Tolerant Layer for Dynamically Reconfigurable Multi-processor System-on-Chip. , 2009, , .		10
9	Designing Efficient Codecs for Bus-Invert Berger Code for Fully Asymmetric Communication. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 777-781.	3.0	10
10	Towards future adaptive multiprocessor systems-on-chip: An innovative approach for flexible architectures. , 2012, , .		10
11	Energy-Efficient GPS Synchronization for Wireless Nodes. IEEE Sensors Journal, 2021, 21, 5221-5229.	4.7	10
12	Real-time scheduling on heterogeneous system-on-chip architectures using an optimised artificial neural network. Journal of Systems Architecture, 2011, 57, 340-353.	4.3	8
13	A Neural Network Model for Real-Time Scheduling on Heterogeneous SoC Architectures. Neural Networks (IJCNN), International Joint Conference on, 2007, , .	0.0	6
14	Flexible communication support for dynamically reconfigurable FPGAS. , 2009, , .		5
15	xMAML: A Modeling Language for Dynamically Reconfigurable Architectures. , 2009, , .		4
16	Reconfigurable ECU communications in Autosar Environment. , 2009, , .		4
17	A new approach of coding to improve speed and noise tolerance of on-chip busses. , 2008, , .		3
18	Communication service for hardware tasks executed on dynamic and partial reconfigurable resources. , 2011, , .		3

#	ARTICLE	IF	CITATIONS
19	Re <sup>2</sup> DA: Reliable and reconfigurable dynamic architecture. , 2011, , .		3
20	Impact of design parameters on performance of adaptive Network-on-Chips. , 2012, , .		3
21	Efficient dynamic reconfiguration for multi-context embedded FPGA. , 2008, , .		2
22	DRAFT: Flexible interconnection network for dynamically reconfigurable architectures. , 2009, , .		2
23	Evaluation of Fault-Mitigation Schemes for Fault-Tolerant Dynamic MPSoC. , 2010, , .		2
24	R2NoC: Dynamically Reconfigurable Routers for Flexible Networks on Chip. , 2010, , .		2
25	Hardware OS Communication Service and Dynamic Memory Management for RSoCs. , 2011, , .		2
26	Cluster based MPSoC architecture: an on-chip message passing implementation. Design Automation for Embedded Systems, 2013, 17, 587-607.	1.0	2
27	FTUC: A Flooding Tree Uneven Clustering Protocol for a Wireless Sensor Network. Sensors, 2017, 17, 2706.	3.8	2
28	Mapping future generation mobile telecommunication applications on a dynamically reconfigurable arcitecture. , 2002, , .		1
29	A Measurement-Based Message-Level Timing Prediction Approach for Data-Dependent SDFGs on Tile-Based Heterogeneous MPSoCs. Applied Sciences (Switzerland), 2021, 11, 6649.	2.5	1
30	Energy- Efficient Reconfigurable Processors. Computer Engineering Series, 2004, , 20-1-20-15.	0.1	1
31	Efficient and Flexible Dynamic Reconfiguration for Multi Context Architectures. Journal of Integrated Circuits and Systems, 2009, 4, 36-44.	0.4	1
32	Spatio-temporal coding to improve speed and noise tolerance of on-chip interconnect. Microelectronics Journal, 2010, 41, 480-486.	2.0	0
33	Comments on "A Low-Power Dependable Berger Code for Fully Asymmetric Communication". IEEE Communications Letters, 2010, 14, 761-763.	4.1	0
34	A framework for the design of reconfigurable fault tolerant architectures. , 2011, , .		0
35	OCEAN, a flexible adaptive Network-On-Chip for dynamic applications. Microprocessors and Microsystems, 2014, 38, 337-357.	2.8	0
36	Du microprocesseur au circuit FPGA. Une analyse sous l'angle de la reconfiguration. Techniques Et Sciences Informatiques, 2005, 24, 395-422.	0.0	0

#	ARTICLE	IF	CITATIONS
37	Architectures reconfigurable et faible consommation. R��alit�� ou prospective ?. Techniques Et Sciences Informatiques, 2007, 26, 595-621.	0.0	0
38	RANN: A Reconfigurable Artificial Neural Network Model for Task Scheduling on��Reconfigurable System-on-Chip. Lecture Notes in Electrical Engineering, 2011, , 117-144.	0.4	0
39	System-Level Modeling and Simulation of MPSoC Run-Time Management Using Execution Traces Analysis. Lecture Notes in Computer Science, 2019, , 281-293.	1.3	0