G Edward Suh

List of Publications by Year in Descending Order

54 papers	1,633 citations	17 h-index	40 g-index
63 ext. papers	2,087 ext. citations	1.4 avg, IF	5.01 L-index

#	Paper	IF	Citations
54	Reverse Engineering CNN Models using Side-Channel Attacks. *IEEE Design and Test*, **2022**, 1-1	1.4	0
53	Sinan: ML-based and QoS-aware resource management for cloud microservices **2021**,		7
52	BCD deduplication: effective memory compression using partial cache-line deduplication **2021**,		1
51	Guessing Outputs of Dynamically Pruned CNNs Using Memory Access Patterns. *IEEE Computer Architecture Letters*, **2021**, 20, 98-101	1.8	
50	. *IEEE Robotics and Automation Letters*, **2020**, 5, 6884-6891	4.2	1
49	TWiCe **2019**,		18
48	Designing Secure Cryptographic Accelerators with Information Flow Enforcement **2019**,		3
47	Boosting the Performance of CNN Accelerators with Dynamic Fine-Grained Channel Gating **2019**,		11
46	TWiCe: Time Window Counter Based Row Refresh to Prevent Row-Hammering. *IEEE Computer Architecture Letters*, **2018**, 17, 96-99	1.8	9
45	FPGA-Based Remote Power Side-Channel Attacks **2018**,		65
44	Reverse engineering convolutional neural networks through side-channel information leaks **2018**,		20
43	High-level synthesis with timing-sensitive information flow enforcement **2018**,		9
42	HyperFlow **2018**,		13
41	An Architectural Framework for Accelerating Dynamic Parallel Algorithms on Reconfigurable Hardware **2018**,		11
40	Reverse Engineering Convolutional Neural Networks Through Side-channel Information Leaks **2018** ,		7
39	Secure Autonomous Cyber-Physical Systems Through Verifiable Information Flow Control **2018**,		3
38	Verification of a Practical Hardware Security Architecture Through Static Information Flow Analysis **2017**,		23

37	Secure Information Flow Verification with Mutable Dependent Types **2017**,		9
36	Verification of a Practical Hardware Security Architecture Through Static Information Flow Analysis. *Operating Systems Review (ACM)*, **2017**, 51, 555-568	0.8	1
35	Verification of a Practical Hardware Security Architecture Through Static Information Flow Analysis. *ACM SIGPLAN Notices*, **2017**, 52, 555-568	0.2	
34	Verification of a Practical Hardware Security Architecture Through Static Information Flow Analysis. *Computer Architecture News*, **2017**, 45, 555-568		6
33	Efficient data supply for hardware accelerators with prefetching and access/execute decoupling **2016**,		8
32	Prediction-Guided Performance-Energy Trade-off with Continuous Run-Time Adaptation **2016**,		5
31	A Hardware Design Language for Timing-Sensitive Information-Flow Security **2015**,		63
30	Prediction-guided performance-energy trade-off for interactive applications **2015**,		20
29	Execution time prediction for energy-efficient hardware accelerators **2015**,		11
28	A Hardware Design Language for Timing-Sensitive Information-Flow Security. *Computer Architecture News*, **2015**, 43, 503-516		12
27	Understanding sources of variations in flash memory for physical unclonable functions **2014**,		10
26	Author retrospective AEGIS **2014**,		4
25	Quadrisection-based task mapping on many-core processors for energy-efficient on-chip communication **2013**,		2
24	. *IEEE Transactions on Computers*, **2013**, 62, 59-73	2.5	15
23	Hiding Information in Flash Memory **2013**,		6
22	Non-race concurrency bug detection through order-sensitive critical sections **2013**,		3
21	Efficient Timing Channel Protection for On-Chip Networks **2012**,		61
20	Worst-case execution time analysis for parallel run-time monitoring **2012**,		2

19	Flash Memory for Ubiquitous Hardware Security Functions: True Random Number Generation and Device Fingerprints **2012**,		65
18	High-performance parallel accelerator for flexible and efficient run-time monitoring **2012**,		19
17	Fast development of hardware-based run-time monitors through architecture framework and high-level synthesis **2012**,		2
16	Precise exception support for decoupled run-time monitoring architectures **2011**,		1
15	Analysis of application-aware on-chip routing under traffic uncertainty **2011**,		3
14	SRAM-DRAM hybrid memory with applications to efficient register files in fine-grained multi-threading **2011**,		38
13	A non-volatile microcontroller with integrated floating-gate transistors **2011**,		26
12	Low power nonvolatile SRAM circuit with integrated low voltage nanocrystal PMOS Flash **2010**,		2
11	Orthrus. *ACM SIGPLAN Notices*, **2010**, 45, 371-384	0.2	0
10	Orthrus **2010**,		8
9	IVEC **2010**,		9
8	Flexible and Efficient Instruction-Grained Run-Time Monitoring Using On-Chip Reconfigurable Fabric **2010**,		41
7	Orthrus. *Computer Architecture News*, **2010**, 38, 371-384		6
6	Hardware authentication leveraging performance limits in detailed simulations and emulations **2009**,		5
5	Static virtual channel allocation in oblivious routing **2009**,		24
4	Physical unclonable functions for device authentication and secret key generation. *Proceedings - Design Automation Conference*, **2007**,		476
3	Aegis: A Single-Chip Secure Processor. *IEEE Design and Test of Computers*, **2007**, 24, 570-580		93
2	Speeding up Exponentiation using an Untrusted Computational Resource. *Designs, Codes, and Cryptography*, **2006**, 39, 253-273	1.2	41

1 Secure program execution via dynamic information flow tracking **2004**, 334