G Edward Suh

List of Publications by Citations

54	1,633	17	40
papers	citations	h-index	g-index
63	2,087	1.4	5.01
ext. papers	ext. citations	avg, IF	L-index

#	Paper	IF	Citations
54	Physical unclonable functions for device authentication and secret key generation. *Proceedings - Design Automation Conference*, **2007**,		476
53	Secure program execution via dynamic information flow tracking **2004**,		334
52	Aegis: A Single-Chip Secure Processor. *IEEE Design and Test of Computers*, **2007**, 24, 570-580		93
51	FPGA-Based Remote Power Side-Channel Attacks **2018**,		65
50	Flash Memory for Ubiquitous Hardware Security Functions: True Random Number Generation and Device Fingerprints **2012**,		65
49	A Hardware Design Language for Timing-Sensitive Information-Flow Security **2015**,		63
48	Efficient Timing Channel Protection for On-Chip Networks **2012**,		61
47	Flexible and Efficient Instruction-Grained Run-Time Monitoring Using On-Chip Reconfigurable Fabric **2010**,		41
46	Speeding up Exponentiation using an Untrusted Computational Resource. *Designs, Codes, and Cryptography*, **2006**, 39, 253-273	1.2	41
45	SRAM-DRAM hybrid memory with applications to efficient register files in fine-grained multi-threading **2011**,		38
44	A non-volatile microcontroller with integrated floating-gate transistors **2011**,		26
43	Static virtual channel allocation in oblivious routing **2009**,		24
42	Verification of a Practical Hardware Security Architecture Through Static Information Flow Analysis **2017**,		23
41	Reverse engineering convolutional neural networks through side-channel information leaks **2018**,		20
40	Prediction-guided performance-energy trade-off for interactive applications **2015**,		20
39	High-performance parallel accelerator for flexible and efficient run-time monitoring **2012**,		19
38	TWiCe **2019**,		18

37	. *IEEE Transactions on Computers*, **2013**, 62, 59-73	2.5	15
36	HyperFlow **2018**,		13
35	A Hardware Design Language for Timing-Sensitive Information-Flow Security. *Computer Architecture News*, **2015**, 43, 503-516		12
34	Boosting the Performance of CNN Accelerators with Dynamic Fine-Grained Channel Gating **2019**,		11
33	Execution time prediction for energy-efficient hardware accelerators **2015**,		11
32	An Architectural Framework for Accelerating Dynamic Parallel Algorithms on Reconfigurable Hardware **2018**,		11
31	Understanding sources of variations in flash memory for physical unclonable functions **2014**,		10
30	Secure Information Flow Verification with Mutable Dependent Types **2017**,		9
29	TWiCe: Time Window Counter Based Row Refresh to Prevent Row-Hammering. *IEEE Computer Architecture Letters*, **2018**, 17, 96-99	1.8	9
28	IVEC **2010**,		9
27	High-level synthesis with timing-sensitive information flow enforcement **2018**,		9
26	Orthrus **2010**,		8
25	Efficient data supply for hardware accelerators with prefetching and access/execute decoupling **2016**,		8
24	Sinan: ML-based and QoS-aware resource management for cloud microservices **2021**,		7
23	Reverse Engineering Convolutional Neural Networks Through Side-channel Information Leaks **2018** ,		7
22	Verification of a Practical Hardware Security Architecture Through Static Information Flow Analysis. *Computer Architecture News*, **2017**, 45, 555-568		6
21	Hiding Information in Flash Memory **2013**,		6
20	Orthrus. *Computer Architecture News*, **2010**, 38, 371-384		6

19	Hardware authentication leveraging performance limits in detailed simulations and emulations **2009**,		5
18	Prediction-Guided Performance-Energy Trade-off with Continuous Run-Time Adaptation **2016**,		5
17	Author retrospective AEGIS **2014**,		4
16	Designing Secure Cryptographic Accelerators with Information Flow Enforcement **2019**,		3
15	Non-race concurrency bug detection through order-sensitive critical sections **2013**,		3
14	Analysis of application-aware on-chip routing under traffic uncertainty **2011**,		3
13	Secure Autonomous Cyber-Physical Systems Through Verifiable Information Flow Control **2018**,		3
12	Quadrisection-based task mapping on many-core processors for energy-efficient on-chip communication **2013**,		2
11	Low power nonvolatile SRAM circuit with integrated low voltage nanocrystal PMOS Flash **2010**,		2
10	Worst-case execution time analysis for parallel run-time monitoring **2012**,		2
9	Fast development of hardware-based run-time monitors through architecture framework and high-level synthesis **2012**,		2
8	Verification of a Practical Hardware Security Architecture Through Static Information Flow Analysis. *Operating Systems Review (ACM)*, **2017**, 51, 555-568	0.8	1
7	Precise exception support for decoupled run-time monitoring architectures **2011**,		1
6	. *IEEE Robotics and Automation Letters*, **2020**, 5, 6884-6891	4.2	1
5	BCD deduplication: effective memory compression using partial cache-line deduplication **2021**,		1
4	Orthrus. *ACM SIGPLAN Notices*, **2010**, 45, 371-384	0.2	0
3	Reverse Engineering CNN Models using Side-Channel Attacks. *IEEE Design and Test*, **2022**, 1-1	1.4	0
2	Verification of a Practical Hardware Security Architecture Through Static Information Flow Analysis. *ACM SIGPLAN Notices*, **2017**, 52, 555-568	0.2	

List of Publications

1	Guessing Outputs of Dynamically Pruned CNNs Using Memory Access Patterns. *IEEE Computer Architecture Letters*, **2021**, 20, 98-101	1.8