Bei Yu

List of Publications by Year
in descending order

200	3,184	394286	360920
papers	citations	19 h-index	35 g-index

203	203	203	1054
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Reliability-Driven Memristive Crossbar Design in Neuromorphic Computing Systems. IEEE Transactions on Automation Science and Engineering, 2023, 20, 74-87.	3.4	1
2	PTPT: Physical Design Tool Parameter Tuning via Multi-Objective Bayesian Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 178-189.	1.9	10
3	McPAT-Calib: A RISC-V BOOM Microarchitecture Power Modeling Framework. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 243-256.	1.9	5
4	A GPU-Enabled Level-Set Method for Mask Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 594-605.	1.9	4
5	Faster Region-Based Hotspot Detection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 669-680.	1.9	9
6	An Efficient Sharing Grouped Convolution via Bayesian Learning. IEEE Transactions on Neural Networks and Learning Systems, 2022, 33, 7367-7379.	7.2	12
7	Deep Learning-Driven Simultaneous Layout Decomposition and Mask Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 709-722.	1.9	4
8	Neural-ILT 2.0: Migrating ILT to Domain-Specific and Multitask-Enabled Neural Network. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2671-2684.	1.9	7
9	Pin-Accessible Legalization for Mixed-Cell-Height Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 143-154.	1.9	10
10	Deep H-GCN: Fast Analog IC Aging-Induced Degradation Estimation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1990-2003.	1.9	10
11	Hotspot Detection via Attention-Based Deep Layout Metric Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2685-2698.	1.9	4
12	High-Speed Adder Design Space Exploration via Graph Neural Processes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2657-2670.	1.9	7
13	MLCAD: A Survey of Research in Machine Learning for CAD Keynote Paper. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3162-3181.	1.9	22
14	Fortune: A New Fault-Tolerance TSV Configuration in Router-Based Redundancy Structure. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3182-3187.	1.9	0
15	DeePattern: Layout Pattern Generation With Transforming Convolutional Auto-Encoder. IEEE Transactions on Semiconductor Manufacturing, 2022, 35, 67-77.	1.4	0
16	Adaptive Layout Decomposition With Graph Embedding Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 5030-5042.	1.9	1
17	Analog Circuit Yield Optimization via Freezeâ€“Thaw Bayesian Optimization Technique. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 4887-4900.	1.9	2
18	Counteracting Adversarial Attacks in Autonomous Driving. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 5193-5206.	1.9	2

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19	Techniques for CAD Tool Parameter Auto-tuning in Physical Synthesis: A Survey (Invited Paper). , 2022, , .		6
20	Efficient Layout Hotspot Detection via Neural Architecture Search. ACM Transactions on Design Automation of Electronic Systems, 2022, 27, 1-16.	1.9	4
21	Correlated Multi-objective Multi-fidelity Optimization for HLS Directives Design. ACM Transactions on Design Automation of Electronic Systems, 2022, 27, 1-27.	1.9	11
22	Efficient Hotspot Detection via Graph Neural Network. , 2022, , .		1
23	Bridging the Gap Between Layout Pattern Sampling and Hotspot Detection via Batch Active Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1464-1475.	1.9	12
24	Efficient Layout Hotspot Detection via Binarized Residual Neural Network Ensemble. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1476-1488.	1.9	7
25	Leveraging Spatial Correlation for Sensor Drift Calibration in Smart Building. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1273-1286.	1.9	5
26	DAC-SDC Low Power Object Detection Challenge for UAV Applications. IEEE Transactions on Pattern Analysis and Machine Intelligence, 2021, 43, 392-403.	9.7	43
27	Correlated Multi-objective Multi-fidelity Optimization for HLS Directives Design. , 2021, , .		17
28	Deep Neural Network Hardware Deployment Optimization via Advanced Active Learning. , 2021, , .		7
29	Towards AQFP-Capable Physical Design Automation. , 2021, , .		3
30	Learning Point Clouds in EDA. , 2021, , .		2
31	Deep Learning Analysis for Split-Manufactured Layouts With Routing Perturbation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1995-2008.	1.9	5
32	Attacking a CNN-based Layout Hotspot Detector Using Group Gradient Method. , 2021, , .		7
33	OpenMPL: An Open-Source Layout Decomposer. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2331-2344.	1.9	7
34	Low-Cost Lithography Hotspot Detection with Active Entropy Sampling and Model Calibration. , 2021, , .		1
35	NeurFill: Migrating Full-Chip CMP Simulators to Neural Networks for Model-Based Dummy Filling Synthesis. , 2021, , .		3
36	Machine Learning in Nanometer AMS Design-for-Reliability : (Invited Paper). , 2021, , .		4

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37	BOOM-Explorer: RISC-V BOOM Microarchitecture Design Space Exploration Framework. , 2021, , .		16
38	Fast and Efficient DNN Deployment via Deep Gaussian Transfer Learning. , 2021, , .		3
39	Graph Learning-Based Arithmetic Block Identification. , 2021, , .		10
40	Hotspot Detection via Multi-task Learning and Transformer Encoder. , 2021, , .		7
41	A Unified Framework for Layout Pattern Analysis with Deep Causal Estimation. , 2021, , .		5
42	AutoGTCO: Graph and Tensor Co-Optimize for Image Recognition with Transformers on GPU. , 2021, , .		3
43	DevelSet: Deep Neural Level Set for Instant Mask Optimization. , 2021, , .		14
44	A High-Performance Accelerator for Super-Resolution Processing on Embedded GPU. , 2021, , .		1
45	Fault tolerance in memristive crossbar-based neuromorphic computing systems. The Integration VLSI Journal, 2020, 70, 70-79.	1.3	12
46	DSA guiding template assignment with multiple redundant via and dummy via insertion. The Integration VLSI Journal, 2020, 70, 32-42.	1.3	0
47	Memristive Crossbar Mapping for Neuromorphic Computing Systems on 3D IC. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-19.	1.9	5
48	SRAF Insertion via Supervised Dictionary Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2849-2859.	1.9	11
49	Reliability-Driven Neural Network Training for Memristive Crossbar-Based Neuromorphic Computing Systems. , 2020, , .		5
50	Deep Learning-Driven Simultaneous Layout Decomposition and Mask Optimization. , 2020, , .		6
51	A Unified Framework for Simultaneous Layout Decomposition and Mask Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5069-5082.	1.9	5
52	GAN-OPC: Mask Optimization With Lithography-Guided Generative Adversarial Nets. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2822-2834.	1.9	42
53	TimingCamouflage+: Netlist Security Enhancement With Unconventional Timing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4482-4495.	1.9	5
54	Cyber-Physical Systems: An Overview. , 2020, , 1-11.		4

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55	Understanding Graphs in EDA. , 2020, , .		21
56	Hotspot detection via attention-based deep layout metric learning. , 2020, , .		22
57	Neural-ILT. , 2020, , .		13
58	DAMO. , 2020, , .		18
59	Adversarial Perturbation Attacks on ML-based CAD. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-31.	1.9	16
60	Smart Building Sensor Drift Calibration. , 2020, , 187-202.		1
61	Reinforcement Learning Driven Physical Synthesis : (Invited Paper). , 2020, , .		2
62	Synergistic Topology Generation and Route Synthesis for On-Chip Performance-Critical Signal Groups. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1147-1160.	1.9	7
63	Layout Hotspot Detection With Feature Tensor Generation and Deep Biased Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1175-1187.	1.9	63
64	A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1585-1598.	1.9	12
65	Sensor Drift Calibration via Spatial Correlation Model in Smart Building. , 2019, , .		7
66	High Performance Graph Convolutional Networks with Applications in Testability Analysis. , 2019, , .		65
67	Attacking Split Manufacturing from a Deep Learning Perspective. , 2019, , .		17
68	SRAF insertion via supervised dictionary learning. , 2019, , .		12
69	Faster Region-based Hotspot Detection. , 2019, , .		30
70	Efficient Layout Hotspot Detection via Binarized Residual Neural Network. , 2019, , .		25
71	DeePattern. , 2019, , .		21
72	FIT. , 2019, , .		10

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73	A local optimal method on DSA guiding template assignment with redundant/dummy via insertion. , 2019, , .		0
74	Hardware-software co-design of slimmed optical neural networks. , 2019, , .		25
75	Detecting multi-layer layout hotspots with adaptive squish patterns. , 2019, , .		19
76	Automatic Layout Generation with Applications in Machine Learning Engine Evaluation. , 2019, , .		7
77	CAD Tool Design Space Exploration via Bayesian Optimization. , 2019, , .		16
78	Congestion-aware Global Routing using Deep Convolutional Generative Adversarial Networks. , 2019, , .		9
79	A Unified Approximation Framework for Compressing and Accelerating Deep Neural Networks. , 2019, , .		4
80	OpenMPL: An Open Source Layout Decomposer: Invited Paper. , 2019, , .		1
81	Power-Driven DNN Dataflow Optimization on FPGA. , 2019, , .		11
82	Cross-Layer Optimization for High Speed Adders: A Pareto Driven Machine Learning Approach. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 2298-2311.	1.9	18
83	Recent advances in convolutional neural network acceleration. Neurocomputing, 2019, 323, 37-51.	3.5	266
84	Provably Secure Camouflaging Strategy for IC Protection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1399-1412.	1.9	32
85	Adaptive 3D-IC TSV Fault Tolerance Structure Generation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 949-960.	1.9	9
86	Hotspot detection using squish-net. , 2019, , .		2
87	MrDP: Multiple-Row Detailed Placement of Heterogeneous-Sized Cells for Advanced Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1237-1250.	1.9	21
88	A practical split manufacturing framework for Trojan prevention via simultaneous wire lifting and cell insertion. , 2018, , .		13
89	A Multicommodity Flow-Based Detailed Router With Efficient Acceleration Techniques. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 217-230.	1.9	17
90	TILA-S: Timing-Driven Incremental Layer Assignment Avoiding Slew Violations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 231-244.	1.9	14

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91	GAN-OPC: Mask Optimization with Lithography-guided Generative Adversarial Nets. , 2018, , .		16
92	Power Grid Reduction by Sparse Convex Optimization. , 2018, , .		2
93	Layout Synthesis for Topological Quantum Circuits With 1-D and 2-D Architectures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1574-1587.	1.9	7
94	RippleFPGA: Routability-Driven Simultaneous Packing and Placement for Modern FPGAs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2022-2035.	1.9	32
95	IEEE Transactions on Sustainable Computing: Guest Editorial on Special Issue on Sustainable Cyber-Physical Systems. IEEE Transactions on Sustainable Computing, 2018, 3, 58-59.	2.2	2
96	GAN-OPC. , 2018, , .		46
97	Routability-driven and fence-aware legalization for mixed-cell-height circuits. , 2018, , .		5
98	Graph-Based Redundant Via Insertion and Guiding Template Assignment for DSA-MP. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2504-2517.	2.1	4
99	TimingCamouflage: Improving circuit security against counterfeiting by unconventional timing. , 2018, , .		29
100	CRMA: Incorporating Cut Redistribution With Mask Assignment to Enable the Fabrication of 1-D Gridded Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2036-2049.	1.9	0
101	Thermal-Aware Placement and Routing for 3D Optical Networks-on-Chips. , 2018, , .		4
102	Sparse VLSI Layout Feature Extraction: A Dictionary Learning Approach. , 2018, , .		11
103	Memristive Crossbar Mapping for Neuromorphic Computing Systems on 3D IC. , 2018, , .		4
104	Triple Patterning Aware Detailed Placement Toward Zero Cross-Row Middle-of-Line Conflict. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1140-1152.	1.9	9
105	Clustered Fault Tolerance TSV Planning for 3-D Integrated Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1287-1300.	1.9	22
106	Stitch aware detailed placement for multiple E-beam lithography. The Integration VLSI Journal, 2017, 58, 47-54.	1.3	11
107	Smart building uncertainty analysis via adaptive Lasso. IET Cyber-Physical Systems: Theory and Applications, 2017, 2, 42-48.	1.9	6
108	Triple/quadruple patterning layout decomposition via linear programming and iterative rounding. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2017, 16, 023507.	1.0	8

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109	Incremental Layer Assignment for Timing Optimization. ACM Transactions on Design Automation of Electronic Systems, 2017, 22, 1-25.	1.9	3
110	Layout Hotspot Detection with Feature Tensor Generation and Deep Biased Learning. , 2017, , .		39
111	Imbalance aware lithography hotspot detection: a deep learning approach. Proceedings of SPIE, 2017, , .	0.8	12
112	DSAR. , 2017, , .		9
113	Bilinear Lithography Hotspot Detection. , 2017, , .		19
114	Incremental Layer Assignment Driven by an External Signoff Timing Engine. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1126-1139.	1.9	4
115	High Performance Dummy Fill Insertion With Coupling and Uniformity Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1532-1544.	1.9	10
116	A learning bridge from architectural synthesis to physical design for exploring power efficient high-performance adders. , 2017, , .		10
117	SD-PUF: Spliced Digital Physical Unclonable Function. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, , 1-1.	1.9	6
118	Clock-aware ultrascale FPGA placement with machine learning routability prediction: (Invited paper). , 2017, , .		32
119	Minimizing Thermal Gradient and Pumping Power in 3D IC Liquid Cooling Network Design. , 2017, , .		8
120	Lithography hotspot detection: From shallow to deep learning. , 2017, , .		27
121	Accelerating chip design with machine learning: From pre-silicon to post-silicon. , 2017, , .		8
122	A unified framework for simultaneous layout decomposition and mask optimization. , 2017, , .		23
123	Methodologies for layout decomposition and mask optimization: A systematic review. , 2017, , .		5
124	Imbalance aware lithography hotspot detection: a deep learning approach. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2017, 16, 1.	1.0	68
125	PARR. ACM Transactions on Design Automation of Electronic Systems, 2016, 21, 1-21.	1.9	24
126	LRR-DPUF. , 2016, , .		7

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127	MrDP. , 2016, , .		18
128	Enabling online learning in lithography hotspot detection with information-theoretic feature optimization. , 2016, , .		61
129	Incorporating cut redistribution with mask assignment to enable 1D gridded design. , 2016, , .		8
130	Provably secure camouflaging strategy for IC protection. , 2016, , .		73
131	VLSI layout hotspot detection based on discriminative feature extraction. , 2016, , .		2
132	Design for manufacturability and reliability in extreme-scaling VLSI. Science China Information Sciences, 2016, 59, 1.	2.7	31
133	Triple/quadruple patterning layout decomposition via novel linear programming and iterative rounding. , 2016, , .		2
134	Optical proximity correction with hierarchical Bayes model. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2016, 15, 021009.	1.0	28
135	Incremental layer assignment for critical path timing. , 2016, , .		12
136	RippleFPGA. , 2016, , .		39
137	Laplacian eigenmaps- and Bayesian clustering-based layout pattern sampling and its applications to hotspot detection and optical proximity correction. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2016, 15, 043504.	1.0	10
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139	MCFRoute 2.0. , 2016, , .		0
140	Laplacian eigenmaps and bayesian clustering based layout pattern sampling and its applications to hotspot detection and OPC. , 2016, , .		4
141	Systematic framework for evaluating standard cell middle-of-line robustness for multiple patterning lithography. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2016, 15, 021202.	1.0	8
142	Concurrent Guiding Template Assignment and Redundant via Insertion for DSA-MP Hybrid Lithography. , 2016, , .		15
143	Layout Decomposition for Other Patterning Techniques. , 2016, , 53-82.		0
144	Design for Manufacturability with E-Beam Lithography. , 2016, , 111-157.		0

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145	Standard Cell Compliance and Placement Co-Optimization. , 2016, , 83-109.		0
146	Conclusions and Future Works. , 2016, , 159-162.		0
147	Layout Decomposition for Triple Patterning. , 2016, , 7-51.		1
148	Layout Decomposition for Triple Patterning. , 2016, , 1062-1065.		0
149	EBL Overlapping Aware Stencil Planning for MCC System. ACM Transactions on Design Automation of Electronic Systems, 2016, 21, 1-24.	1.9	2
150	Triple patterning aware detailed placement toward zero cross-row middle-of-line conflict. , 2015, , .		7
151	Electromigration-aware redundant via insertion. , 2015, , .		12
152	Optical proximity correction with hierarchical Bayes model. Proceedings of SPIE, 2015, , .	0.8	18
153	TILA: Timing-driven incremental layer assignment. , 2015, , .		8
154	High performance dummy fill insertion with coupling and uniformity constraints. , 2015, , .		9
155	Standard Cell Layout Regularity and Pin Access Optimization Considering Middle-of-Line. , 2015, , .		30
156	Self-Aligned Double Patterning Aware Pin Access and Standard Cell Layout Co-Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 699-712.	1.9	38
157	Methodology for Standard Cell Compliance and Detailed Placement for Triple Patterning Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 726-739.	1.9	33
158	Layout Decomposition for Triple Patterning Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 433-446.	1.9	54
159	Machine learning and pattern matching in physical design. , 2015, , .		29
160	A systematic framework for evaluating standard cell middle-of-line (MOL) robustness for multiple patterning. Proceedings of SPIE, 2015, , .	0.8	2
161	Directed Self-Assembly Based Cut Mask Optimization for Unidirectional Design. , 2015, , .		15
162	PARR. , 2015, , .		21

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163	Pushing multiple patterning in sub-10nm. , 2015, , .		26
164	Directed self-assembly cut mask assignment for unidirectional design. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2015, 14, 031211.	1.0	19
165	A new lithography hotspot detection framework based on AdaBoost classifier and simplified feature extraction. Proceedings of SPIE, 2015, , .	0.8	25
166	Self-aligned double patterning aware pin access and standard cell layout co-optimization. , 2014, , .		22
167	MOSAIC. , 2014, , .		55
168	Layout Decomposition for Quadruple Patterning Lithography and Beyond. , 2014, , .		20
169	Layout compliance for triple patterning lithography: an iterative approach. , 2014, , .		2
170	Accurate lithography hotspot detection based on PCA-SVM classifier with hierarchical data clustering. Proceedings of SPIE, 2014, , .	0.8	12
171	Accurate lithography hotspot detection based on principal component analysis-support vector machine classifier with hierarchical data clustering. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2014, 14, 011003.	1.0	34
172	Triple patterning lithography layout decomposition using end-cutting. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2014, 14, 011002.	1.0	12
173	Self-aligned double patterning layout decomposition with complementary e-beam lithography. , 2014, , .		15
174	MOSAIC: Mask optimizing solution with process window aware inverse correction. , 2014, , .		5
175	Layout decomposition for quadruple patterning lithography and beyond. , 2014, , .		8
176	Bridging the gap from mask to physical design for multiple patterning lithography. Proceedings of SPIE, 2014, , .	0.8	0
177	Design for Manufacturing With Emerging Nanolithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1453-1472.	1.9	100
178	Lithography hotspot detection and mitigation in nanometer VLSI. , 2013, , .		2
179	E-BLOW. , 2013, , .		16
180	Methodology for standard cell compliance and detailed placement for triple patterning lithography. , 2013, , .		27

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181	L-shape based layout fracturing for e-beam lithography. , 2013, , .		3
182	A high-performance triple patterning layout decomposer with balanced density. , 2013, , .		35
183	A mixed sample-time error calibration technique in time-interleaved ADCs. IEICE Electronics Express, 2013, 10, 20130882-20130882.	0.3	9
184	Triple patterning lithography (TPL) layout decomposition using end-cutting. Proceedings of SPIE, 2013, , .	0.8	14
185	Self-aligned double patterning friendly configuration for standard cell library considering placement impact. Proceedings of SPIE, 2013, , .	0.8	8
186	<title>Implications of triple patterning for 14nm node design and patterning</title>. , 2012, , .		28
187	TRIAD. , 2012, , .		38
188	A 14-bit 200-MS/s time-interleaved ADC with sample-time error calibration. Journal of Semiconductors, 2012, 33, 105010.	2.0	2
189	Dealing with IC manufacturability in extreme scaling. , 2012, , .		19
190	GLOW: A global router for low-power thermal-reliable interconnect synthesis using photonic wavelength multiplexing. , 2012, , .		25
191	EPIC: Efficient prediction of IC manufacturing hotspots with a unified meta-classification formulation. , 2012, , .		58
192	E-Beam Lithography Stencil Planning and Optimization With Overlapped Characters. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 167-179.	1.9	32
193	Cluster Generation and Network Component Insertion for Topology Synthesis of Application-Specific Network-on-Chips. IEICE Transactions on Electronics, 2012, E95.C, 534-545.	0.3	5
194	Layout decomposition for triple patterning lithography. , 2011, , .		75
195	Application-specific Network-on-Chip synthesis: Cluster generation and network component insertion. , 2011, , .		16
196	Network flow-based simultaneous retiming and slack budgeting for low power design. , 2011, , .		1
197	Floorplanning and topology generation for application-specific Network-on-Chip. , 2010, , .		7
198	Multi-voltage and level-shifter assignment driven floorplanning. , 2009, , .		5

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199	Voltage-island driven floorplanning considering level-shifter positions. , 2009, , .		10
200	Voltage and Level-Shifter Assignment Driven Floorplanning. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 2990-2997.	0.2	6