Ji-zhong Shen

List of Publications by Year
in descending order

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35 papers	494 citations	1307594 7 h-index	677142 22 g-index
35 all docs	35 docs citations	35 times ranked	428 citing authors

#	Article	IF	Citations
1	Localization of seizure onset zone with epilepsy propagation networks based on graph convolutional network. Biomedical Signal Processing and Control, 2022, 74, 103489.	5.7	1
2	An Automatic HFO Detection Method Combining Visual Inspection Features with Multi-Domain Features. Neuroscience Bulletin, 2021, 37, 777-788.	2.9	7
3	Low-rate DoS attack detection method based on hybrid deep neural networks. Journal of Information Security and Applications, 2021, 60, 102879.	2.5	6
4	EPILEPTIC EEG IDENTIFICATION BASED ON HYBRID FEATURE EXTRACTION. Journal of Mechanics in Medicine and Biology, 2020, 20, 2050025.	0.7	6
5	Web page classification based on heterogeneous features and a combination of multiple classifiers. Frontiers of Information Technology and Electronic Engineering, 2020, 21, 995-1004.	2.6	6
6	A Method of Few-Shot Network Intrusion Detection Based on Meta-Learning Framework. IEEE Transactions on Information Forensics and Security, 2020, 15, 3540-3552.	6.9	114
7	P300-based deception detection of mock network fraud with modified genetic algorithm and combined classification. , 2019, , .		0
8	An Intrusion Detection System Using a Deep Neural Network With Gated Recurrent Units. IEEE Access, 2018, 6, 48697-48707.	4.2	192
9	Dynamic current mode logic based flipâ€flop design for robust and lowâ€power security integrated circuits. Electronics Letters, 2017, 53, 1236-1238.	1.0	8
10	Transistor level SCA-resistant scheme based on fluctuating power logic. Science China Information Sciences, 2017, 60, 1.	4.3	2
11	Function synthesis algorithm based on RTD-based three-variable universal logic gates. Frontiers of Information Technology and Electronic Engineering, 2017, 18, 1654-1664.	2.6	2
12	An algorithm for identifying symmetric variables based on the order eigenvalue matrix. Frontiers of Information Technology and Electronic Engineering, 2017, 18, 1644-1653.	2.6	0
13	Improved low-entropy masking scheme for LED with mitigation against correlation-enhanced collision attacks. , 2017, , .		1
14	An Algorithm for Identifying Symmetric Variables in the Canonical Reedâ€“Muller Algebra System. Journal of Circuits, Systems and Computers, 2016, 25, 1650126.	1.5	1
15	Power-efficient dual-edge implicit pulse-triggered flip-flop with an embedded clock-gating scheme. Frontiers of Information Technology and Electronic Engineering, 2016, 17, 962-972.	2.6	5
16	P300â€based deception detection in simulated network fraud condition. Electronics Letters, 2016, 52, 1136-1138.	1.0	2
17	Design of flipâ€flops with clockâ€gating and pullâ€up control scheme for powerâ€constrained and speedâ€insensitive applications. IET Computers and Digital Techniques, 2016, 10, 193-201.	1.2	7
18	Low Power Pulse-Triggered Flip-Flop Based on Clock Triggering Edge Control Technique. Journal of Circuits, Systems and Computers, 2015, 24, 1550094.	1.5	2

#	Article	IF	Citations
19	Design of a novel RTD-based three-variable universal logic gate. Frontiers of Information Technology and Electronic Engineering, 2015, 16, 694-699.	2.6	2
20	Function Synthesis Algorithm of RTD-Based Universal Threshold Logic Gate. Journal of Applied Mathematics, 2015, 2015, 1-7.	0.9	0
21	A dynamic submatrix-based P300 online brainâ€“computer interface. Biomedical Signal Processing and Control, 2015, 15, 27-32.	5.7	7
22	An algorithm for identifying symmetric variables in the canonical OR-coincidence algebra system. Journal of Zhejiang University: Science C, 2014, 15, 1174-1182.	0.7	0
23	Research of P300 Feature Extraction Algorithm Based on ICA and Wavelet Transform. , 2014, , .		6
24	Design of ternary clock generator. Electronics Letters, 2014, 50, 1052-1054.	1.0	2
25	A Graph Route-Based Superframe Scheduling Scheme in WirelessHART Mesh Networks for High Robustness. Wireless Personal Communications, 2013, 71, 2431-2444.	2.7	34
26	A general structure of all-edges-triggered flip-flop based on multivalued clock. International Journal of Electronics, 2013, 100, 1637-1645.	1.4	4
27	Low-power explicit-pulsed triggered flipâ€“flop with robust output. Electronics Letters, 2012, 48, 1523-1525.	1.0	4
28	A submatrix-based P300 brain-computer interface stimulus presentation paradigm. Journal of Zhejiang University: Science C, 2012, 13, 452-459.	0.7	25
29	Design of nanopipelined adder based on resonant tunneling diode. Microelectronics Journal, 2012, 43, 353-357.	2.0	3
30	Design of a novel low power 8-transistor 1-bit full adder cell. Journal of Zhejiang University: Science C, 2011, 12, 604-607.	0.7	17
31	Novel universal threshold logic gate based on RTD and its application. Microelectronics Journal, 2011, 42, 851-854.	2.0	15
32	Structure and design method for pulse-triggered flip-flops at switch level. Central South University, 2010, 17, 1279-1284.	0.5	7
33	An explicit-pulsed double-edge triggered JK flip-flop. , 2009, , .		6
34	The structure of dynamic BiCMOS circuit and its switch-level design. , 2008, , .		0
35	Circuit implementation of multi-thresholded neuron (MTN) using BiCMOS technology. , 0, , .		0