Hsiang-Yun Cheng

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/6694528/publications.pdf

Version: 2024-02-01

18	362	1937685 4	1872680 6
papers	citations	h-index	g-index

18	18	18	373
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	DL-RSIM: A Reliability and Deployment Strategy Simulation Framework for ReRAM-based CNN Accelerators. Transactions on Embedded Computing Systems, 2022, 21, 1-29.	2.9	4
2	This is SPATEM! A Spatial-Temporal Optimization Framework for Efficient Inference on ReRAM-based CNN Accelerator. , 2022, , .		1
3	Future Computing Platform Design: A Cross-Layer Design Approach. , 2021, , .		6
4	RePIM: Joint Exploitation of Activation and Weight Repetitions for In-ReRAM DNN Acceleration. , 2021, , .		5
5	ReSpar: Reordering Algorithm for ReRAM-based Sparse Matrix-Vector Multiplication Accelerator. , 2021, , .		0
6	GraphRSim: A Joint Device-Algorithm Reliability Analysis for ReRAM-based Graph Processing. , 2020, , .		3
7	Sparse ReRAM engine. , 2019, , .		121
8	TAP: Reducing the Energy of Asymmetric Hybrid Last-Level Cache via Thrashing Aware Placement and Migration. IEEE Transactions on Computers, 2019, 68, 1704-1719.	3.4	7
9	DL-RSIM. , 2018, , .		50
10	Improving GPGPU Performance via Cache Locality Aware Thread Block Scheduling. IEEE Computer Architecture Letters, 2017, 16, 127-131.	1.5	12
11	LAP: Loop-Block Aware Inclusion Properties for Energy-Efficient Asymmetric Last Level Caches. , 2016, , .		6
12	Designs of emerging memory based non-volatile TCAM for Internet-of-Things (IoT) and big-data processing: A 5T2R universal cell. , 2016, , .		23
13	LAP. Computer Architecture News, 2016, 44, 103-114.	2.5	9
14	Core vs. uncore. , 2015, , .		27
15	EECache. Transactions on Architecture and Code Optimization, 2015, 12, 1-22.	2.0	44
16	Adaptive Burst-Writes (ABW). ACM Transactions on Design Automation of Electronic Systems, 2015, 21, 1-26.	2.6	2
17	EECache. , 2014, , .		8
18	Memory Latency Reduction via Thread Throttling. , 2010, , .		34