## Hsiang-Yun Cheng

List of Publications by Year in descending order

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1937685 1872680 18 362 4 6 citations g-index h-index papers 18 18 18 373 docs citations times ranked citing authors all docs

#	Article	IF	CITATIONS
1	Sparse ReRAM engine., 2019,,.		121
2	DL-RSIM., 2018,,.		50
3	EECache. Transactions on Architecture and Code Optimization, 2015, 12, 1-22.	2.0	44
4	Memory Latency Reduction via Thread Throttling. , 2010, , .		34
5	Core vs. uncore., 2015,,.		27
6	Designs of emerging memory based non-volatile TCAM for Internet-of-Things (IoT) and big-data processing: A 5T2R universal cell. , $2016$ , , .		23
7	Improving GPGPU Performance via Cache Locality Aware Thread Block Scheduling. IEEE Computer Architecture Letters, 2017, 16, 127-131.	1.5	12
8	LAP. Computer Architecture News, 2016, 44, 103-114.	2.5	9
9	EECache., 2014,,.		8
10	TAP: Reducing the Energy of Asymmetric Hybrid Last-Level Cache via Thrashing Aware Placement and Migration. IEEE Transactions on Computers, 2019, 68, 1704-1719.	3.4	7
11	LAP: Loop-Block Aware Inclusion Properties for Energy-Efficient Asymmetric Last Level Caches., 2016,,.		6
12	Future Computing Platform Design: A Cross-Layer Design Approach., 2021,,.		6
13	RePIM: Joint Exploitation of Activation and Weight Repetitions for In-ReRAM DNN Acceleration. , 2021, , .		5
14	DL-RSIM: A Reliability and Deployment Strategy Simulation Framework for ReRAM-based CNN Accelerators. Transactions on Embedded Computing Systems, 2022, 21, 1-29.	2.9	4
15	GraphRSim: A Joint Device-Algorithm Reliability Analysis for ReRAM-based Graph Processing. , 2020, , .		3
16	Adaptive Burst-Writes (ABW). ACM Transactions on Design Automation of Electronic Systems, 2015, 21, 1-26.	2.6	2
17	This is SPATEM! A Spatial-Temporal Optimization Framework for Efficient Inference on ReRAM-based CNN Accelerator., 2022,,.		1
18	ReSpar: Reordering Algorithm for ReRAM-based Sparse Matrix-Vector Multiplication Accelerator. , 2021, , .		0