Sandeep Saini

List of Publications by Year
in descending order

36 papers	**306** citations

2258059
3 h-index

1588992
8 g-index

38 all docs	**38** docs citations

38 times ranked

116 citing authors

#	Article	IF	Citations
1	Hardware–Software Co-Design Framework for Data Encryption in Image Processing Systems for the Internet of Things Environment. IEEE Consumer Electronics Magazine, 2022, 11, 92-97.	2.3	4
2	Stock values predictions using deep learning based hybrid models. CAAI Transactions on Intelligence Technology, 2022, 7, 107-116.	8.1	31
3	Stock Market Predictions Using FastRNN-Based Model. Advances in Intelligent Systems and Computing, 2022, , 439-450.	0.6	1
4	A novel model based on Sequential Adaptive Memory for English–Hindi Translation. Cognitive Computation and Systems, 2021, 3, 142-153.	1.4	3
5	Stock Market Predictions Using FastRNN, CNN, and Bi-LSTM-Based Hybrid Model. Lecture Notes in Electrical Engineering, 2021, , 1-10.	0.4	1
6	Cognitive architecture for natural language comprehension. Cognitive Computation and Systems, 2020, 2, 23-31.	1.4	8
7	Language learnability analysis of Hindi: a comparison with ideal and constrained learning approaches. , 2020, , 273-290.		0
8	Setting up a neural machine translation system for English to Indian languages. , 2020, , 195-212.		5
9	Bi-LSTM and Ensemble based Bilingual Sentiment Analysis for a Code-mixed Hindi-English Social Media Text. , 2020, , .		13
10	Hardware Software Co-Simulation of an AES-128 based Data Encryption in Image Processing Systems for the Internet of Things Environment. , 2020, , .		7
11	Bilingual Sentiment Analysis for a Code-mixed Punjabi English Social Media Text. , 2020, , .		13
12	Language Learnability Analysis of Hindi: A Comparison with Ideal and Constrained Learning Approaches. Journal of Psycholinguistic Research, 2019, 48, 947-960.	1.3	1
13	Neural Machine Translation for English to Hindi. , 2018, , .		30
14	Securing qr codes by rsa on fpga. , 2017, , .		4
15	A hybrid approach to emotion recognition system using multi-discriminant analysis & k-nearest neighbour. , 2017, , .		3
16	A Quadro Coding Technique to Reduce Self Transitions in VLSI Interconnects. , 2016, , .		6
17	Bayesian learner based language learnability analysis of Hindi. , 2016, , .		2
18	FPGA based hardware implementation of automatic vehicle license plate detection system. , 2016, , .		9

#	ARTICLE	IF	CITATIONS
19	Low Power Interconnect Design. , 2015, , .		9
20	Relative clause based text simplification for improved English to Hindi translation. , 2015, , .		5
21	A Survey of Machine Translation Techniques and Systems for Indian Languages. , 2015, , .		33
22	Parity Preserving Adder/Subtractor Using a Novel Reversible Gate. , 2015, , .		2
23	User Interactive and Assistive Fleet Management and Eco-Driving System. , 2015, , .		3
24	A novel design of reversible 2:4 decoder. , 2015, , .		15
25	Buffer Insertion as a Solution to Interconnect Issues. , 2015, , 57-74.		1
26	Thermometer to Gray Encoders. Advances in Computer and Electrical Engineering Book Series, 2015, , 323-335.	0.3	3
27	A novel design of compact reversible SG gate and its applications. , 2014, , .		12
28	High speed convolution and deconvolution algorithm (Based on Ancient Indian Vedic Mathematics). , 2014, , .		7
29	A 4-bit, 3.2 GSPS flash analog to digital converter with a new multiplexer based encoder. , 2014, , .		6
30	Binary division algorithm and high speed deconvolution algorithm (Based on Ancient Indian Vedic) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50		10
31	Design of low power and high speed multiplexer based Thermometer to Gray encoder. , 2013, , .		12
32	A new bus coding technique to minimize crosstalk in VLSI bus. , 2011, , .		6
33	An Alternative approach to Buffer Insertion for Delay and Power Reduction in VLSI Interconnects. , 2010, , .		12
34	Implementation of low power FFT structure using a method based on conditionally coded blocks. , 2010, , .		4
35	An Alternate Approach to Buffer Insertion for Delay and Power Reduction in VLSI Interconnects. Journal of Low Power Electronics, 2010, 6, 429-435.	0.6	0
36	Schmitt trigger as an alternative to buffer insertion for delay and power reduction in VLSI interconnects. , 2009, , .		25