Chrysostomos Nicopoulos

List of Publications by Year
in descending order

63	1,459	687363 13	434195 31
papers	citations	h-index	g-index

68	68	68	743
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Low-Cost Online Convolution Checksum Checker. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 201-212.	3.1	6
2	Autonomous Application of Netlist Transformations Inside Lagrangian Relaxation-Based Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1672-1686.	2.7	5
3	Timing-Driven Placement Optimization Facilitated by Timing-Compatibility Flip-Flop Clustering. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2835-2848.	2.7	9
4	The Mesochronous Dual-Clock FIFO Buffer. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 302-306.	3.1	9
5	A Hardware-assisted Heartbeat Mechanism for Fault Identification in Large-scale IoT Systems. IEEE Transactions on Dependable and Secure Computing, 2020, , 1-1.	5.4	9
6	Practical Verifiable Computation by Using a Hardware-Based Correct Execution Environment. IEEE Access, 2020, 8, 216689-216706.	4.2	3
7	Design Optimization by Fine-grained Interleaving of Local Netlist Transformations in Lagrangian Relaxation. , 2020, , .		3
8	Dynamic Adjustment of Test-Sequence Duration for Increasing the Functional Coverage. , 2019, , .		0
9	Multi-Armed Bandits for Autonomous Timing-driven Design Optimization. , 2019, , .		5
10	Automatic Generation of Peak-Power Traffic for Networks-on-Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 96-108.	2.7	4
11	Hardware-Based Online Self-Diagnosis for Faulty Device Identification in Large-Scale IoT Systems. , 2018, , .		4
12	Low-power dual-edge-triggered synchronous latency-insensitive systems. , 2018, , .		1
13	A Dual-Clock Multiple-Queue Shared Buffer. IEEE Transactions on Computers, 2017, 66, 1809-1815.	3.4	10
14	Networks-on-Chip With Double-Data-Rate Links. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 3103-3114.	5.4	14
15	RapidLink: A network-on-chip architecture with double-data-rate links. , 2016, , .		1
16	Powermax: an automated methodology for generating peak-power traffic in networks-on-chip. , 2016, , .		2
17	A Low-Power Network-on-Chip Architecture for Tile-based Chip Multi-Processors. , 2016, , .		13
18	An Online and Real-Time Fault Detection and Localization Mechanism for Network-on-Chip Architectures. Transactions on Architecture and Code Optimization, 2016, 13, 1-26.	2.0	10

#	Article	IF	Citations
19	ShortPath: A Network-on-Chip Router with Fine-Grained Pipeline Bypassing. IEEE Transactions on Computers, 2016, 65, 3136-3147.	3.4	25
20	PhaseNoC: Versatile Network Traffic Isolation Through TDM-Scheduled Virtual Channels. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 844-857.	2.7	13
21	Toward Multi-Layer Holistic Evaluation of System Designs. IEEE Computer Architecture Letters, 2016, 15, 58-61.	1.5	1
22	Subtleties of Run-Time Virtual Address Stacks. IEEE Computer Architecture Letters, 2015, 14, 152-155.	1.5	0
23	Timing-resilient Network-on-Chip architectures. , 2015, , .		1
24	HARPA: Solutions for dependable performance under physically induced performance variability. , 2015, , .		2
25	ElastiStore: Flexible Elastic Buffering for Virtual-Channel-Based Networks on Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 3015-3028.	3.1	19
26	Size-Aware Cache Management for Compressed Cache Architectures. IEEE Transactions on Computers, 2015, 64, 2337-2352.	3.4	9
27	Designing Hybrid DRAM/PCM Main Memory Systems Utilizing Dual-Phase Compression. ACM Transactions on Design Automation of Electronic Systems, 2014, 20, 1-31.	2.6	21
28	Centaur: a hybrid network-on-chip architecture utilizing micro-network fusion. Design Automation for Embedded Systems, 2014, 18, 121-139.	1.0	2
29	Sharded Router: A novel on-chip router architecture employing bandwidth sharding and stealing. Parallel Computing, 2013, 39, 372-388.	2.1	2
30	IsoNet: Hardware-Based Job Queue Management for Many-Core Architectures. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1080-1093.	3.1	12
31	Dynamic faultâ€tolerant routing algorithm for networksâ€onâ€chip based on localised detouring paths. IET Computers and Digital Techniques, 2013, 7, 93-103.	1.2	13
32	Do we need wide flits in Networks-on-Chip?. , 2013, , .		30
33	TornadoNoC. Transactions on Architecture and Code Optimization, 2013, 10, 1-30.	2.0	6
34	ECM: Effective Capacity Maximizer for high-performance compressed caching. , 2013, , .		16
35	Hardware-Assisted Intrusion Detection by Preserving Reference Information Integrity. Lecture Notes in Computer Science, 2013, , 291-300.	1.3	0
36	A programmable processing array architecture supporting dynamic task scheduling and module-level prefetching. , 2012, , .		2

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37	Optimizing Data-Center TCO with Scale-Out Processors. IEEE Micro, 2012, 32, 52-63.	1.8	32
38	A Dynamically Adjusting Gracefully Degrading Link-Level Fault-Tolerant Mechanism for NoCs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1235-1248.	2.7	23
39	Virtualizing Virtual Channels for Increased Network-on-Chip Robustness and Upgradeability. , 2012, , .		19
40	Thermal characterization of cloud workloads on a power-efficient server-on-chip. , 2012, , .		18
41	NoCAlert: An On-Line and Real-Time Fault Detection Mechanism for Network-on-Chip Architectures. , 2012, , .		71
42	A highly robust distributed fault-tolerant routing algorithm for NoCs with localized rerouting. , 2012, , .		6
43	A Compression-Based Hybrid MLC/SLC Management Technique for Phase-Change Memory Systems. , 2012, , .		24
44	A dual-phase compression mechanism for hybrid DRAM/PCM main memory architectures. , 2012, , .		14
45	Large-Scale Semantic Concept Detection on Manycore Platforms for Multimedia Mining. , 2011, , .		4
46	Hardware-Based Job Queue Management for Manycore Architectures and OpenMP Environments. , 2011, , .		3
47	An energy- and performance-aware DRAM cache architecture for hybrid DRAM/PCM main memory systems. , 2011, , .		41
48	Variation-Aware Task and Communication Mapping for MPSoC Architecture. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 295-307.	2.7	27
49	A High-Performance and Energy-Efficient Virtually Tagged Stack Cache Architecture for Multi-core Environments. , 2011, , .		2
50	On the Effects of Process Variation in Network-on-Chip Architectures. IEEE Transactions on Dependable and Secure Computing, 2010, 7, 240-254.	5.4	50
51	A fine-grained link-level fault-tolerant mechanism for networks-on-chip. , 2010, , .		10
52	Field Programmable Compressor Trees. ACM Transactions on Reconfigurable Technology and Systems, 2009, 2, 1-36.	2.5	9
53	Performance and power optimization through data compression in Network-on-Chip architectures. High Performance Computer Architecture (HPCA), Proceedings of the IEEE International Symposium on, 2008, , .	0.0	56
54	Analysis and solutions to issue queue process variation. , 2008, , .		3

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55	Design space exploration for field programmable compressor trees. , 2008, , .		2
56	Variation-Aware Low-Power Buffer Design. Conference Record of the Asilomar Conference on Signals, Systems and Computers, 2007, , .	0.0	6
57	A novel dimensionally-decomposed router for on-chip communication in 3D architectures. , 2007, , .		168
58	Design of a Dynamic Priority-Based Fast Path Architecture for On-Chip Interconnects. , 2007, , .		19
59	Design of a Dynamic Priority-Based Fast Path Architecture for On-Chip Interconnects. , 2007, , .		5
60	ViChaR: A Dynamic Virtual Channel Regulator for Network-on-Chip Routers. Microarchitecture (MICRO), Proceedings of the Annual International Symposium on, 2006, , .	0.0	172
61	A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks. Computer Architecture News, 2006, 34, 4-15.	2.5	131
62	A Distributed Multi-Point Network Interface for Low-Latency, Deadlock-Free On-Chip Interconnects. , 2006, , .		14
63	Design and Management of 3D Chip Multiprocessors Using Network-in-Memory. Computer Architecture News, 2006, 34, 130-141.	2.5	244