Bogdan Majkusiak

List of Publications by Year in descending order

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65	537	949033 11	799663 21
papers	citations	h-index	g-index

67	67	67	336
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Charge-Trapping-Induced Hysteresis Effects in Highly Doped Silicon Metalâ€“Oxideâ€“Semiconductor Structures. Materials, 2022, 15, 2733.	1.3	1
2	Investigation of Electrical Properties of the Al/SiO2/n++-Si Resistive Switching Structures by Means of Static, Admittance, and Impedance Spectroscopy Measurements. Materials, 2021, 14, 6042.	1.3	8
3	Modeling the Currentâ€“Voltage Characteristics of Geâ‚‚â‚‹â‚“Snâ‚“ Electronâ€“Hole Bilayer TFET With Various Compositions. IEEE Transactions on Electron Devices, 2020, 67, 2738-2744.	1.6	2
4	Frequency Modulated C-V Characteristics Shift in Double-layer High-k Gate Stack MIS Devices. , 2020, , .		1
5	Tunneling and Resonant Tunneling Effects in the Metal-Ultrathin Oxide-(n+)Silicon Structures. , 2020, , .		1
6	Effect of traps-to-gate tunnel communication on C-V characteristics of MIS capacitors. Microelectronic Engineering, 2019, 215, 111011.	1.1	0
7	Modeling the Tunnel Field-Effect Transistor Based on Different Tunneling Path Approaches. IEEE Transactions on Electron Devices, 2018, 65, 2626-2631.	1.6	11
8	Simulations of transient processes and characteristics of the nc-MOS structures. Microelectronic Engineering, 2017, 178, 173-177.	1.1	2
9	Technology and characterization of MIS structures with co-doped silicon nanocrystals (Si-NCs) embedded in hafnium oxide (HfOx) ultra-thin layers. Microelectronic Engineering, 2017, 178, 298-303.	1.1	9
10	Charging/discharging processes in nanocrystaline MOS structures - Theoretical study. Journal of Physics: Conference Series, 2016, 709, 012012.	0.3	4
11	Effect of nanocrystal geometric location on tunnel currents and smallâ€signal admittance of MIS structures. Physica Status Solidi C: Current Topics in Solid State Physics, 2016, 13, 1035-1039.	0.8	3
12	Effect of interface traps parameters on admittance characteristics of the MIS (metal-insulator-semiconductor) tunnel structures. Proceedings of SPIE, 2016, , .	0.8	0
13	Modeling of tunnel field effect transistor: the impact of construction parameters. , 2016, , .		0
14	Effect of inner interface traps on high-k gate stack admittance characteristics. , 2016, , .		1
15	Reactive Ion Etching (RIE) of silicon for the technology of nanoelectronic devices and structures. Proceedings of SPIE, 2016, , .	0.8	0
16	Impact of nanocrystal(s) location on C-V-t and I-V-t characteristics of ncMOS structures. , 2016, , .		1
17	Small-signal admittance model of multi-traps distributed over energy and space in the insulator of MIS tunnel structures. Microelectronic Engineering, 2015, 147, 349-353.	1.1	6
18	Study of the effect of tunneling through the traps inside the insulator on small-signal admittance of the MOS structure. Microelectronic Engineering, 2013, 109, 1-4.	1.1	2

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19	Small-signal admittance model as a characterization tool of the MOS tunnel diode. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2013, 31, 01A111.	0.6	10
20	Investigation of current-voltage characteristics of the transistor structures with double-potential barrier DBMOS. , 2013, , .		0
21	Investigation of temperature effect on electrical characteristics of the double barrier metal-oxide-semiconductor structure. , 2013, , .		0
22	Modeling the current of a double-gate MOSFET with very thin active region taking into account mobility dependence on the transverse electric field. Proceedings of SPIE, 2013, , .	0.8	0
23	Description of tunneling through a metal-insulator-metal junction considering Coulomb Blockade. , 2013, , .		0
24	WKB approximation based formula for tunneling probability through a multi-layer potential barrier. , 2012, , .		1
25	Investigation of double barrier MOS tunnel diodes with PECVD silicon quantum well. Microelectronics Reliability, 2011, 51, 1172-1177.	0.9	4
26	Modeling of tunneling through a three-layer gate stack with/without a quantum well. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2011, 29, .	0.6	4
27	Drain current computation in nanoscale nMOSFETs: Comparison of transport models. , 2010, , .		0
28	Analytical modeling of the tunneling probability through the double-layer gate stacks. Journal of Vacuum Science & Technology B, 2009, 27, 346.	1.3	6
29	A comparison of advanced transport models for the computation of the drain current in nanoscale nMOSFETs. Solid-State Electronics, 2009, 53, 1293-1302.	0.8	18
30	Comparison of advanced transport models for nanoscale nMOSFETs. , 2009, , .		1
31	Physics of the Multigate MOS System. , 2008, , 155-189.		1
32	Theoretical Study of Electron Mobility in Double-Gate Field Effect Transistors with Multilayer (strained-)Si/SiGe Channel. Journal of Semiconductor Technology and Science, 2008, 8, 264-275.	0.1	4
33	Transport and quantum scattering time in field-effect transistors. Applied Physics Letters, 2007, 90, 172104.	1.5	8
34	Electron Mobility and Concentration on Submicrometer Scale â€" Investigation of Si and AlGaN/GaN Field Effect Transistors by AC Magnetoresistance Method. AIP Conference Proceedings, 2007, , .	0.3	0
35	Comparison of Modeling Approaches for the Capacitanceâ€“Voltage and Currentâ€“Voltage Characteristics of Advanced Gate Stacks. IEEE Transactions on Electron Devices, 2007, 54, 106-114.	1.6	27
36	Modeling the Inelastic Scattering Effect on the Resonant Tunneling Current. Journal of Computational Electronics, 2007, 6, 207-210.	1.3	4

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37	Resonant Tunneling Devices on SOI Basis. NATO Science for Peace and Security Series B: Physics and Biophysics, 2007, , 341-356.	0.2	3
38	Simulation of the gate tunnel current in the double gate (DG) MOS transistor. Journal of Computational Electronics, 2006, 5, 143-148.	1.3	7
39	Theoretical Limit for the SiO2 Thickness in Silicon MOS Devices. , 2005, , 309-320.		2
40	Comparison of resonant tunneling currents in double gate MOS diodes with metal and poly-silicon gates. Microelectronic Engineering, 2004, 72, 96-100.	1.1	0
41	MOVPE Deposition of AlAs/In0.53Ga0.47As/InP Resonant Tunneling Heterostructure Performing High PVR Parameter. Journal of Wide Bandgap Materials, 2001, 9, 93-100.	0.1	0
42	The remote roughness mobility resulting from the ultrathin SiO2 thickness nonuniformity in the DG SOI and bulk MOS transistors. Microelectronic Engineering, 2001, 59, 417-421.	1.1	9
43	Quantum-mechanical effects in SOI devices. Solid-State Electronics, 2001, 45, 607-611.	0.8	1
44	Semiconductor thickness and back-gate voltage effects on the gate tunnel current in the MOS/SOI system with an ultrathin oxide. IEEE Transactions on Electron Devices, 2000, 47, 2347-2351.	1.6	7
45	Theory of the MOS/SOI tunnel diode. Microelectronic Engineering, 1999, 48, 375-378.	1.1	1
46	Semiconductor thickness effects in the double-gate SOI MOSFET. IEEE Transactions on Electron Devices, 1998, 45, 1127-1134.	1.6	81
47	Analysis of the MOS transistor based on the self-consistent solution to the Schrodinger and Poisson equations and on the local mobility model. IEEE Transactions on Electron Devices, 1998, 45, 1263-1271.	1.6	70
48	Experimental and theoretical study of the current-voltage characteristics of the MISIM tunnel transistor. IEEE Transactions on Electron Devices, 1998, 45, 1903-1911.	1.6	15
49	Electron energy quantization effects in the very thin film GAA SOI transistor. Microelectronic Engineering, 1997, 36, 379-382.	1.1	4
50	Influence of carrier energy quantization on the gate-induced drain breakdown. Solid-State Electronics, 1995, 38, 1933-1936.	0.8	0
51	Influence of carrier energy quantization on threshold voltage of metalâ€oxideâ€semiconductor transistor. Journal of Applied Physics, 1994, 75, 5186-5190.	1.1	26
52	Influence of oxide thickness nonuniformities on the tunnel currentâ€voltage and capacitanceâ€voltage characteristics of the metalâ€oxideâ€semiconductor system. Journal of Applied Physics, 1993, 74, 5638-5647.	1.1	33
53	A technical formula for determining the insulator capacitance in a MOS structure. Solid-State Electronics, 1992, 35, 223-224.	0.8	16
54	A review of long-channel MOS transistor models. Microelectronics Journal, 1991, 22, 55-88.	1.1	0

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55	Gate tunnel current in an MOS transistors. IEEE Transactions on Electron Devices, 1990, 37, 1087-1092.	1.6	43
56	Analytical modelling of long-channel MOSFET Iâ€“V characteristics with improved accuracy. Microelectronics Journal, 1990, 21, 23-28.	1.1	0
57	Very thin oxides in vlsi technology: Properties and device implications. Microelectronics Journal, 1990, 21, 21-40.	1.1	3
58	Influence of highâ€dose Î³ irradiation on electron mobility in a silicon inversion layer. Applied Physics Letters, 1990, 57, 1643-1644.	1.5	3
59	Series resistance in a MOS capacitor with a thin gate oxide. Solid-State Electronics, 1989, 32, 137-140.	0.8	26
60	The initial growth rate of thermal silicon oxide. Physica Status Solidi A, 1989, 116, 313-329.	1.7	10
61	A modified method for determination of surface mobility of carriers in MOS transistors. Physica Status Solidi A, 1989, 116, 833-836.	1.7	2
62	A new method for the simultaneous determination of the surface-carrier mobility and the metal-semiconductor work-function difference in MOS transistors. IEEE Transactions on Electron Devices, 1988, 35, 439-443.	1.6	4
63	The influence of degeneracy in the channel on long-channel MOSFET characteristics. IEEE Transactions on Electron Devices, 1987, 34, 2560-2561.	1.6	5
64	The dependence of MOSFET surface carrier mobility on gate-oxide thickness. IEEE Transactions on Electron Devices, 1986, 33, 1717-1721.	1.6	7
65	On electron tunneling in the metalâ€insulatorâ€semiconductor systems including various electron effective masses. Journal of Applied Physics, 1985, 58, 3141-3144.	1.1	17