Hailong Yao

List of Publications by Year
in descending order

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62 papers	728 citations	949033 11 h-index	993246 17 g-index
62 all docs	62 docs citations	62 times ranked	278 citing authors

#	Article	IF	Citations
1	Contamination-Aware Synthesis for Programmable Microfluidic Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 5016-5029.	1.9	1
2	DCSA: Distributed Channel-Storage Architecture for Flow-Based Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 115-128.	1.9	18
3	Predicting the fluid behavior of random microfluidic mixers using convolutional neural networks. Lab on A Chip, 2021, 21, 296-309.	3.1	20
4	Automated calibration of 3D-printed microfluidic devices based on computer vision. Biomicrofluidics, 2021, 15, 024102.	1.2	6
5	Splitter-Aware Multiterminal Routing With Length-Matching Constraint for RSFQ Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2251-2264.	1.9	4
6	Integrated Control-Fluidic Codesign Methodology for Paper-Based Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 613-625.	1.9	5
7	URBER: Ultrafast Rule-Based Escape Routing Method for Large-Scale Sample Delivery Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 157-170.	1.9	5
8	Microfluidic Design for Concentration Gradient Generation Using Artificial Neural Network. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2544-2557.	1.9	12
9	Multicontrol: Advanced Control-Logic Synthesis for Flow-Based Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2489-2502.	1.9	19
10	Lookup Table-Based Fast Reliability-Aware Sample Preparation Using Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2708-2721.	1.9	5
11	Transfer Learning-Based Microfluidic Design System for Concentration Generation. , 2020, , .		1
12	TAEM: Fast Transfer-Aware Effective Loop Mapping for Heterogeneous Resources on CGRA. , 2020, , .		10
13	Automatic Breast Cancer Grading of Histological Images using Dilated Residual Network. , 2019, , .		2
14	Design Methodology for TFT-Based Pseudo-CMOS Logic Array With Multilayer Interconnection Architecture and Optimization Algorithms. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 2043-2057.	1.9	1
15	Earlyâ€stage microfluidic network design framework using graph sparsificiation based optimisation. Electronics Letters, 2019, 55, 1034-1037.	0.5	0
16	AARF: Any-Angle Routing for Flow-Based Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 3042-3055.	1.9	12
17	Multi-channel and fault-tolerant control multiplexing for flow-based microfluidic biochips. , 2018, , .		16
18	A Comprehensive Security System for Digital Microfluidic Biochips. , 2018, , .		10

#	Article	IF	Citations
19	Physical Co-Design of Flow and Control Layers for Flow-Based Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1157-1170.	1.9	25
20	More Effective Randomly-Designed Microfluidics. , 2018, , .		2
21	Hamming-distance-based valve-switching optimization for control-layer multiplexing in flow-based microfluidic biochips. , 2017, , .		19
22	Close-to-optimal placement and routing for continuous-flow microfluidic biochips. , 2017, , .		45
23	Design Methodology for Thin-Film Transistor Based Pseudo-CMOS Logic Array with Multi-Layer Interconnect Architecture. , 2017, , .		2
24	Pressure-Aware Control Layer Optimization for Flow-Based Microfluidic Biochips. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 1488-1499.	2.7	14
25	Transport or Store?. , 2017, , .		19
26	LUTOSAP. , 2017, , .		10
27	Integrated Functional and Washing Routing Optimization for Cross-Contamination Removal in Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1283-1296.	1.9	22
28	Sequence-pair-based placement and routing for flow-based microfluidic biochips. , 2016, , .		5
29	Integrated Flow-Control Codesign Methodology for Flow-Based Microfluidic Biochips. IEEE Design and Test, 2015, 32, 60-68.	1.1	32
30	PACOR. , 2015, , .		33
31	Obstacle-Avoiding and Slew-Constrained Clock Tree Synthesis With Efficient Buffer Insertion. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 142-155.	2.1	19
32	Practical functional and washing droplet routing for cross-contamination avoidance in digital microfluidic biochips. , 2014, , .		3
33	Fast and scalable parallel layout decomposition in double patterning lithography. The Integration VLSI Journal, 2014, 47, 175-183.	1.3	4
34	Length matching in detailed routing for analog and mixed signal circuits. Microelectronics Journal, 2014, 45, 604-612.	1.1	1
35	SUALD: Spacing uniformity-aware layout decomposition in triple patterning lithography. , 2013, , .		12
36	Analog routing considering min-area constraint. , 2013, , .		0

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37	FaSEA: Fast single-trunk detailed router for electromigration avoidance. , 2013, , .		1
38	A new splitting graph construction algorithm for SIAR router. , 2013, , .		2
39	WIPAL: Window-based parallel layout decomposition in double patterning lithography. , 2012, , .		3
40	LEMAR: A novel length matching routing algorithm for analog and mixed signal circuits. , 2012, , .		16
41	A novel fine-grain track routing approach for routability and crosstalk optimization. , 2011, , .		2
42	Minimization of Circuit Delay and Power through Gate Sizing and Threshold Voltage Assignment. , 2011, , .		7
43	TIPO: A heuristic algorithm for delay constrained power optimization. , 2011, , .		0
44	A novel detailed routing algorithm with exact matching constraint for analog and mixed signal circuits. , 2011, , .		9
45	Analog circuit shielding routing algorithm based on net classification. , 2010, , .		14
46	Layout Decomposition Approaches for Double Patterning Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 939-952.	1.9	74
47	Dose Map and Placement Co-Optimization for Improved Timing Yield and Leakage Power. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1070-1082.	1.9	1
48	Revisiting the linear programming framework for leakage power vs. performance optimization. , 2009, , .		16
49	Congestion-driven multilevel full-chip routing framework. Tsinghua Science and Technology, 2008, 13, 843-849.	4.1	0
50	Efficient range pattern matching algorithm for process-hotspot detection. IET Circuits, Devices and Systems, 2008, 2, 2.	0.9	15
51	Layout decomposition for double patterning lithography. , 2008, , .		78
52	On modeling and sensitivity of via count in SOC physical implementation. , 2008, , .		4
53	Dose map and placement co-optimization for timing yield enhancement and leakage power reduction. , 2008, , .		6
54	Revisiting the layout decomposition problem for double patterning lithography. , 2008, , .		11

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55	CMP-aware Maze Routing Algorithm for Yield Enhancement. , 2007, , .		5
56	DFM-aware Routing for Yield Enhancement. , 2006, , .		2
57	Crosstalk-Aware Routing Resource Assignment. Journal of Computer Science and Technology, 2005, 20, 231-236.	0.9	2
58	Improved multilevel routing with redundant via placement for yield and reliability. , 2005, , .		37
59	Congestion and performance driven full-chip scalable routing framework. , 2005, , .		0
60	Cross point assignment algorithm with crosstalk constraint. , 2003, , .		1
61	Crosstalk driven routing resource assignment. , 0, , .		5
62	Congestion-driven W-shape Multilevel Full-chip Routing Framework. , 0, , .		3