Yarui Peng

List of Publications by Year
in descending order

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46 papers	395 citations	1307594 7 h-index	996975 15 g-index
46 all docs	46 docs citations	46 times ranked	286 citing authors

#	Article	IF	Citations
1	Holistic and In-Context Design Flow for 2.5D Chiplet-Package Interaction Co-Optimization. , 2021, , .		0
2	Holistic Chipletâ€“Package Co-Optimization for Agile Custom 2.5-D Design. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11, 715-726.	2.5	5
3	PowerSynth-Guided Reliability Optimization of Multi-Chip Power Module. , 2021, , .		1
4	Cross-Boundary Inductive Timing Optimization for 2.5D Chiplet-Package Co-Design. , 2021, , .		1
5	PowerSynth Integrated CAD flow for High Density Power Modules. , 2021, , .		3
6	Placement and Routing for Power Module Layout. , 2021, , .		4
7	PowerSynth Design Automation Flow for Hierarchical and Heterogeneous 2.5-D Multichip Power Modules. IEEE Transactions on Power Electronics, 2021, 36, 8919-8933.	7.9	21
8	A Scalable In-Context Design and Extraction Flow for Heterogeneous 2.5D Chiplet-Package Co-Optimization. , 2021, , .		0
9	Fast and Accurate Inductance Extraction for Power Module Layout Optimization Using Loop-Based Method. , 2021, , .		3
10	Hierarchical Layout Synthesis and Optimization Framework for High-Density Power Module Design Automation. , 2021, , .		1
11	Impact of reimbursement rates on the length of stay in tertiary public hospitals: a retrospective cohort study in Shenzhen, China. BMJ Open, 2020, 10, e040066.	1.9	0
12	PowerSynth progression on layout optimization for reliability and signal integrity. Nonlinear Theory and Its Applications IEICE, 2020, 11, 124-144.	0.6	2
13	The Increasing Role of Design Automation in Power Electronics: Gathering What Is Needed. IEEE Power Electronics Magazine, 2020, 7, 46-50.	0.7	31
14	Chiplet-Package Co-Design For 2.5D Systems Using Standard ASIC CAD Tools. , 2020, , .		12
15	Coupling extraction and optimization for heterogeneous 2.5D chiplet-package co-design. , 2020, , .		5
16	Holistic 2.5D Chiplet Design Flow: A 65nm Shared-Block Microcontroller Case Study. , 2020, , .		0
17	General Equation to Determine Design Rules for Mitigating Partial Discharge and Electrical Breakdown in Power Module Layouts. , 2020, , .		1
18	Physical Design Automation for High-Density 3D Power Module Layout Synthesis and Optimization. , 2020, , .		4

#	Article	IF	Citations
19	Electronic Design Automation (EDA) Tools and Considerations for Electro-Thermo-Mechanical Co-Design of High Voltage Power Modules. , 2020, , .		10
20	PEEC Method and Hierarchical Approach Towards 3D Multichip Power Module (MCPM) Layout Optimization. , 2019, , .		11
21	Hierarchical Layout Synthesis and Design Automation for 2.5D Heterogeneous Multi-Chip Power Modules. , 2019, , .		4
22	PowerSynth: A Power Module Layout Generation Tool. IEEE Transactions on Power Electronics, 2019, 34, 5063-5078.	7.9	49
23	System-Level Thermal Management and Reliability of Automotive Electronics: Goals and Opportunities in the Next Generation of Electric and Hybrid Electric Vehicles. , 2019, , .		1
24	Development of EDA Techniques for Power Module EMI Modeling and Layout Optimization. International Symposium on Microelectronics, 2019, 2019, 000193-000198.	0.0	5
25	Interdie Coupling Extraction and Physical Design Optimization for Face-to-Face 3-D ICs. IEEE Nanotechnology Magazine, 2018, 17, 634-644.	2.0	3
26	Toward Partial Discharge Reduction by Corner Correction in Power Module Layouts. , 2018, , .		14
27	Constraint-Aware Algorithms for Heterogeneous Power Module Layout Synthesis and Reliability Optimization. , 2018, , .		6
28	Design Methodologies for Low-Power 3-D ICs With Advanced Tier Partitioning. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2109-2117.	3.1	12
29	Parasitic Extraction for Heterogeneous Face-to-Face Bonded 3-D ICs. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2017, 7, 912-924.	2.5	7
30	Residual Stress and Pop-Out Simulation for TSVs and Contacts in Via-Middle Process. IEEE Transactions on Semiconductor Manufacturing, 2017, 30, 143-154.	1.7	5
31	Chip/package co-analysis and inductance extraction for fan-out wafer-level-packaging. , 2017, , .		3
32	Response surface modeling for parasitic extraction for multi-objective optimization of multi-chip power modules (MCPMs). , 2017, , .		11
33	Die-to-package coupling extraction for fan-out wafer-level-packaging. , 2017, , .		1
34	Full-Chip Signal Integrity Analysis and Optimization of 3-D ICs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1636-1648.	3.1	22
35	3D IC power benefit study under practical design considerations. , 2015, , .		2
36	Fine-Grained 3-D IC Partitioning Study With a Multicore Processor. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2015, 5, 1393-1401.	2.5	4

#	Article	IF	Citations
37	Thermal impact study of block folding and face-to-face bonding in 3D IC. , 2015, , .		4
38	Multi-TSV and E-Field Sharing Aware Full-chip Extraction and Mitigation of TSV-to-Wire Coupling. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1964-1976.	2.7	6
39	Full-chip inter-die parasitic extraction in face-to-face-bonded 3D ICs. , 2015, , .		4
40	Ultralow Power Circuit Design With Subthreshold/Near-Threshold 3-D IC Technologies. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2015, 5, 980-990.	2.5	5
41	Design, packaging, and architectural policy co-optimization for DC power integrity in 3D DRAM. , 2015, , .		7
42	On Enhancing Power Benefits in 3D ICs. , 2014, , .		26
43	Silicon Effect-Aware Full-Chip Extraction and Mitigation of TSV-to-TSV Coupling. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1900-1913.	2.7	32
44	Full-chip multiple TSV-to-TSV coupling extraction and optimization in 3D ICs. , 2013, , .		30
45	Design and analysis of ultra low power processors using sub/near-threshold 3D stacked ICs. , 2013, , .		2
46	On accurate full-chip extraction and optimization of TSV-to-TSV coupling elements in 3D ICs. , 2013, , .		15