Teruki Someya

List of Publications by Year
in descending order

14 papers	180 citations	1307594 7 h-index	1474206 9 g-index
14 all docs	14 docs citations	14 times ranked	189 citing authors

#	Article	IF	Citations
1	A Ka-Band SATCOM Transceiver in 65-nm CMOS With High-Linearity TX and Dual-Channel Wide-Dynamic-Range RX for Terrestrial Terminal. IEEE Journal of Solid-State Circuits, 2022, 57, 356-370.	5.4	9
2	A 0.37mm² Fully-Integrated Wide Dynamic Range Sub-GHz Receiver Front-end without Off-chip Matching Components. IEICE Transactions on Electronics, 2022, , .	0.6	1
3	A Fully Synthesizable Fractional-N MDLL With Zero-Order Interpolation-Based DTC Nonlinearity Calibration and Two-Step Hybrid Phase Offset Calibration. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 603-616.	5.4	27
4	A Low-Jitter Injection-Locked Clock Multiplier Using 97-Î¼W Transformer-Based VCO with 18-kHz Flicker Noise Corner. IEICE Transactions on Electronics, 2021, E104.C, .	0.6	1
5	A 6.4 nW 1.7% Relative Inaccuracy CMOS Temperature Sensor Utilizing Sub-Thermal Drain Voltage Stabilization and Frequency-Locked Loop. IEEE Solid-State Circuits Letters, 2020, 3, 458-461.	2.0	13
6	A CMOS Ka-Band SATCOM Transceiver with ACI-Cancellation Enhanced Dual-Channel Low-NF Wide-Dynamic-Range RX and High-Linearity TX. , 2020, , .		7
7	A Compact TF-Based LC-VCO with Ultra-Low-Power Operation and Supply Pushing Reduction for IoT Applications. IEICE Transactions on Electronics, 2020, E103.C, 505-513.	0.6	0
8	An HDL-described Fully-synthesizable Sub-GHz IoT Transceiver with Ring Oscillator based Frequency Synthesizer and Digital Background EVM Calibration. , 2019, , .		13
9	A 265-mu W Fractional-${N}$ Digital PLL With Seamless Automatic Switching Sub-Sampling/Sampling Feedback Path and Duty-Cycled Frequency-Locked Loop in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2019, 54, 3478-3492.	5.4	29
10	An 11-nW CMOS Temperature-to-Digital Converter Utilizing Sub-Threshold Current at Sub-Thermal Drain Voltage. IEEE Journal of Solid-State Circuits, 2019, 54, 613-622.	5.4	49
11	A 0.4-ps-Jitter â^'52-dBc-Spur Synthesizable Injection-Locked PLL With Self-Clocked Nonoverlap Update and Slope-Balanced Subsampling BBPD. IEEE Solid-State Circuits Letters, 2019, 2, 5-8.	2.0	12
12	A 78 fs RMS Jitter Injection-Locked Clock Multiplier Using Transformer-Based Ultra-Low-Power VCO. , 2019, , .		2
13	A 0.90â€“4.39-V Detection Voltage Range, 56-Level Programmable Voltage Detector Using Fine Voltage-Step Subtraction for Battery Management. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 1270-1279.	5.4	10
14	56-Level programmable voltage detector in steps of 50mV for battery management. , 2016, , .		7