Edith Beigne

List of Publications by Year
in descending order

77	932	687363 13	580821 25
papers	citations	h-index	g-index

79	79	79	795
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Illusion of large on-chip memory by networked computing chips for neural network inference. Nature Electronics, 2021, 4, 71-80.	26.0	15
2	Fine-Grain Back Biasing for the Design of Energy-Quality Scalable Operators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1042-1055.	2.7	2
3	A 50.5 ns Wake-Up-Latency 11.2 pJ/Inst Asynchronous Wake-Up Controller in FDSOI 28 nm. Journal of Low Power Electronics and Applications, 2019, 9, 8.	2.0	3
4	Resistive RAM Endurance: Array-Level Characterization and Correction Techniques Targeting Deep Learning Applications. IEEE Transactions on Electron Devices, 2019, 66, 1281-1288.	3.0	43
5	Misalignment Analysis and Electrical Performance of High Density 3D-IC interconnects. , 2019, , .		4
6	Resistive RAM With Multiple Bits Per Cell: Array-Level Demonstration of 3 Bits Per Cell. IEEE Transactions on Electron Devices, 2019, 66, 641-646.	3.0	43
7	A 5500-frames/s 85-GOPS/W 3-D Stacked BSI Vision Chip Based on Parallel In-Focal-Plane Acquisition and Processing. IEEE Journal of Solid-State Circuits, 2019, 54, 1096-1105.	5.4	18
8	1.45-fJ/bit Access Two-Port SRAM Interfacing a Synchronous/Asynchronous IoT Platform for Energy-Efficient Normally Off Applications. IEEE Solid-State Circuits Letters, 2018, 1, 186-189.	2.0	3
9	High-Density 4T SRAM Bitcell in 14-nm 3-D CoolCube Technology Exploiting Assist Techniques. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2296-2306.	3.1	12
10	A 32 kb 0.35â€“1.2 V, 50 MHzâ€“2.5 GHz Bit-Interleaved SRAM With 8 T SRAM Cell and Data Dependent Write Assist in 28-nm UTBB-FDSOI CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2438-2447.	5.4	12
11	A methodology for the design of dynamic accuracy operators by runtime back bias. , 2017, , .		7
12	AES Datapath Optimization Strategies for Low-Power Low-Energy Multisecurity-Level Internet-of-Things Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3281-3290.	3.1	60
13	Innovative structures to test bonding alignment and characterize high density interconnects in 3D-IC. , 2017, , .		6
14	In-situ Fmax/Vmin tracking for energy efficiency and reliability optimization. , 2017, , .		4
15	Architecture exploration of a fixed point computation unit using precise timing spiking neurons. , 2017, , .		0
16	Ultra Low Energy FDSOI Asynchronous Reconfiguration Network for Adaptive Circuits. Journal of Low Power Electronics and Applications, 2017, 7, 11.	2.0	0
17	Energy-Efficient Near-Threshold Parallel Computing: The PULPv2 Cluster. IEEE Micro, 2017, 37, 20-31.	1.8	58
18	A 128x128, 34Î¼m pitch, 8.9mW, 190mK NETD, TECless Uncooled IR bolometer image sensor with column-wise processing. IS&T International Symposium on Electronic Imaging, 2017, 2017, 68-73.	0.4	1

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19	Adaptive Architectures, Circuits and Technology Solutions for Future IoT Systems. Journal of Low Power Electronics, 2017, 13, 298-309.	0.6	0
20	An SEU tolerant MRAM based non-volatile asynchronous circuit design. , 2016, , .		2
21	Three-Independent-Gate Transistors: Opportunities in digital, analog and RF applications. , 2016, , .		9
22	Ultra low energy FDSOI asynchronous reconfiguration network for an IoT wireless sensor network node. , 2016, , .		2
23	Ultra low-power and low-energy 32-bit datapath AES architecture for IoT applications. , 2016, , .		15
24	Asynchronous Circuit Designs for the Internet of Everything: A Methodology for Ultralow-Power Circuits with GALS Architecture. IEEE Solid-State Circuits Magazine, 2016, 8, 39-47.	0.4	19
25	UTBB FDSOI suitability for IoT applications: Investigations at device, design and architectural levels. Solid-State Electronics, 2016, 125, 14-24.	1.4	5
26	Tracking BTI and HCI effects at circuit-level in adaptive systems. , 2016, , .		0
27	Impact of the AER-induced timing distortion on Spiking Neural Networks implementing DSP. , 2016, , .		2
28	Emerging nano-devices for IOT applications. , 2016, , .		1
29	8.1 a 4x4x2 homogeneous scalable 3d network-on-chip circuit with 326mflit/s 0.66pj/b robust and fault-tolerant asynchronous 3d links. , 2016, , .		13
30	Body Bias usage in UTBB FDSOI designs: A parametric exploration approach. Solid-State Electronics, 2016, 117, 138-145.	1.4	12
31	Dedicated network for distributed configuration in a mixed-signal Wireless Sensor Node circuit. , 2015, , .		1
32	Unified Power Format (UPF) methodology in a vendor independent flow. , 2015, , .		6
33	Evaluation and mitigation of aging effects on a digital on-chip voltage and temperature sensor. , 2015, , .		1
34	A 460 MHz at 397 mV, 2.6 GHz at 1.3 V, 32 bits VLIW DSP Embedding F MAX Tracking. IEEE Journal of Solid-State Circuits, 2015, 50, 125-136.	5.4	42
35	Magnetic Random Access Memory based non-volatile asynchronous Muller cell for ultra-low power autonomous applications. Journal of Applied Physics, 2015, 117, 17B517.	2.5	1
36	A Survey on Low-Power Techniques with Emerging Technologies. ACM Journal on Emerging Technologies in Computing Systems, 2015, 12, 1-26.	2.3	16

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37	Power gain estimation of an event-driven wake-up controller dedicated to WSN's microcontroller. , 2015, , .		1
38	Radiative Effects on MRAM-Based Non-Volatile Elementary Structures. , 2015, , .		4
39	FIFO-level-based power management and its application to an H.264 encoder. , 2014, , .		0
40	H.264/AVC hardware encoders and low-power features. , 2014, , .		3
41	A 460MHz at 397mV, 2.6GHz at 1.3V, 32b VLIW DSP, embedding F_{MAX} tracking. , 2014, , .		29
42	Power management through DVFS and dynamic body biasing in FD-SOI circuits. , 2014, , .		6
43	A Fine-Grain Variation-Aware Dynamic <formula formulatype="inline"><tex Notation="TeX">${m Vdd}$</tex></formula>-Hopping AVFS Architecture on a 32 nm GALS MPSoC. IEEE Journal of Solid-State Circuits, 2014, 49, 1475-1486.	5.4	22
44	Dynamic Variability Monitoring Using Statistical Tests for Energy Efficient Adaptive Architectures. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1741-1754.	5.4	5
45	Power management through DVFS and dynamic body biasing in FD-SOI circuits. , 2014, , .		2
46	Automatic Leakage Control for Wide Range Performance QDI Asynchronous Circuits in FD-SOI Technology. , 2013, , .		12
47	Hardware implementation for entropy coding and byte stream packing engine in H.264/AVC. , 2013, , .		4
48	Low-Cost Dynamic Voltage and Frequency Management Based upon Robust Control Techniques under Thermal Constraints. Lecture Notes in Computer Science, 2013, , 334-353.	1.3	2
49	Fine grain multi-V<inf>T</inf> co-integration methodology in UTBB FD-SOI technology. , 2013, , .		10
50	Local environmental variability monitoring using hypothesis tests. , 2012, , .		1
51	A Pseudo-Synchronous Implementation Flow for WCHB QDI Asynchronous Circuits. , 2012, , .		30
52	Statistical leakage estimation in 32nm CMOS considering cells correlations. , 2012, , .		0
53	Local Condition Monitoring in integrated circuits using a set of Kolmogorov-Smirnov tests. , 2012, , .		0
54	Statistical Estimation of Dominant Physical Parameters for Leakage Variability in 32 Nanometer CMOS, Under Supply Voltage Variations. Journal of Low Power Electronics, 2012, 8, 113-124.	0.6	0

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55	An innovative local adaptive voltage scaling architecture for on-chip variability compensation. , 2011, , .		14
56	Bringing Robustness and Power Efficiency to Autonomous Energy-Harvesting Microsystems. IEEE Design and Test of Computers, 2011, 28, 84-94.	1.0	13
57	Low-Cost and Robust Control of a DFLL for Multi-Processor System-on-Chip. IFAC Postprint Volumes IPPV / International Federation of Automatic Control, 2011, 44, 1940-1945.	0.4	7
58	Timing slack monitoring under process and environmental variations: Application to a DSP performance optimization. Microelectronics Journal, 2011, 42, 718-732.	2.0	12
59	Architecture and Robust Control of a Digital Frequency-Locked Loop for Fine-Grain Dynamic Voltage and Frequency Scaling in Globally Asynchronous Locally Synchronous Structures. Journal of Low Power Electronics, 2011, 7, 328-340.	0.6	12
60	On Line Power Optimization of Data Flow Multi-core Architecture Based on Vdd-Hopping for Local DVFS. Lecture Notes in Computer Science, 2011, , 94-104.	1.3	3
61	On-line Power Optimization of Data Flow Multi-Core Architecture Based on Vdd-Hopping for Local Dynamic Voltage and Frequency Scaling. Journal of Low Power Electronics, 2011, 7, 265-273.	0.6	2
62	CMOS Logic Gates Leakage Modeling Under Statistical Process Variations. Lecture Notes in Electrical Engineering, 2010, , 191-202.	0.4	0
63	An On-Chip Multi-mode Buck DC-DC Converter for Fine-Grain DVS on a Multi-power Domain SoC Using a 65-nm Standard CMOS Logic Process. Lecture Notes in Computer Science, 2010, , 336-346.	1.3	0
64	An On-Chip Multi-Mode Buck DCâ€“DC Converter for Fine-Grain DVS on a Multi-Power Domain SoC Using a 65-nm Standard CMOS Logic Process. Journal of Low Power Electronics, 2010, 6, 201-210.	0.6	0
65	An asynchronous low-power innovative network-On-chip including design-for-test capabilities. , 2009, , .		0
66	On-chip DC-DC converter for IP-level dynamic voltage scaling. , 2009, , .		1
67	Power Reduction of Asynchronous Logic Circuits Using Activity Detection. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 893-906.	3.1	14
68	An accurate approach for statistical estimation of leakage current considering multi-parameter process variations in nanometer CMOS technologies. , 2009, , .		5
69	A 65-nm on-chip multi-mode asynchronous local power supply unit for multi-power domain SoCs achieving fine grain DVS. , 2009, , .		1
70	Design and Implementation of a GALS Adapter for ANoC Based Architectures. , 2009, , .		44
71	An Asynchronous Power Aware and Adaptive NoC Based Circuit. IEEE Journal of Solid-State Circuits, 2009, 44, 1167-1177.	5.4	83
72	A Reconfigurable Baseband Platform Based on an Asynchronous Network-on-Chip. IEEE Journal of Solid-State Circuits, 2008, 43, 223-235.	5.4	64

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73	Automatic Gate Biasing of an SCCMOS Power Switch Achieving Maximum Leakage Reduction and Lowering Leakage Current Variability. IEEE Journal of Solid-State Circuits, 2008, 43, 1688-1698.	5.4	21
74	Statistical leakage modeling in CMOS logic gates considering process variations. , 2008, , .		7
75	Automatic Power Regulation Based on an Asynchronous Activity Detection and its Application to ANOC Node Leakage Reduction. , 2008, , .		15
76	A Telecom Baseband Circuit based on an Asynchronous Network-on-Chip. , 2007, , .		36
77	Gate bias circuit for an SCCMOS power switch achieving maximum leakage reduction. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2007, , .	0.0	5