Chiu-Sing Choy

List of Publications by Year
in descending order

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97	688	1039406	839053
papers	citations	9 h-index	18 g-index

97	97	97	510
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	An efficient MFCC extraction method in speech recognition. , 0, , .		112
2	Reversed nested miller compensation with voltage buffer and nulling resistor. IEEE Journal of Solid-State Circuits, 2003, 38, 1735-1738.	3.5	76
3	A Five-Stage Pipeline, 204 Cycles/MB, Single-Port SRAM-Based Deblocking Filter for H.264/AVC. IEEE Transactions on Circuits and Systems for Video Technology, 2008, 18, 363-374.	5.6	52
4	Hardware Design of Real Time Epileptic Seizure Detection Based on STFT and SVM. IEEE Access, 2018, 6, 67277-67290.	2.6	38
5	Deep sparse rectifier neural networks for speech denoising. , 2016, , .		32
6	A Power-Efficient and Self-Adaptive Prediction Engine for H.264/AVC Decoding. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 302-313.	2.1	28
7	A Low-Power Continuously-Calibrated Clock Recovery Circuit for UHF RFID EPC Class-1 Generation-2 Transponders. IEEE Journal of Solid-State Circuits, 2010, 45, 587-599.	3.5	24
8	A Fully Differential Band-Selective Low-Noise Amplifier for MB-OFDM UWB Receivers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 653-657.	2.2	22
9	A low-latency NoC router with lookahead bypass. , 2010, , .		18
10	Design of passive UHF RFID tag in 130nm CMOS technology. , 2008, , .		14
11	Architecture and Design Flow for a Highly Efficient Structured ASIC. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 424-433.	2.1	14
12	A 1.2 V 900 MHz CMOS mixer. , 0, , .		13
13	An HMM-based speech recognition IC. , 0, , .		13
14	A 5.4-mW 180-cm Transmission Distance 2.5-Mb/s Advanced Techniques-Based Novel Intrabody Communication Receiver Analog Front End. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2829-2841.	2.1	13
15	A new control circuit for asynchronous micropipelines. IEEE Transactions on Computers, 2001, 50, 992-997.	2.4	12
16	An I/Q Mismatch-Free Switched-Capacitor Complex Sigmaâ€“Delta Modulator. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2004, 51, 254-256.	2.3	12
17	A 90nm RFID tag's baseband processor with novel PIE decoder and uplink clock generator. , 2010, , .		11
18	Adiabatic Smart Card. , 2006, , .		9

#	Article	IF	Citations
19	A low voltage current mode CMOS integrated receiver front-end for GPS system. Analog Integrated Circuits and Signal Processing, 2010, 63, 23-31.	0.9	9
20	High speed CMOS digital-to-analog converter with linear interpolator. IEEE Transactions on Consumer Electronics, 2000, 46, 1137-1142.	3.0	8
21	A 75-dB Image Rejection IF-Input Quadrature-Sampling SC<tex>$SigmaDelta$</tex>Modulator. IEEE Journal of Solid-State Circuits, 2006, 41, 1353-1363.	3.5	8
22	An ALU design using a novel asynchronous pipeline architecture. , 0, , .		7
23	A low power asynchronous GF(2/sup 173/) ALU for elliptic curve crypto-processor. , 0, , .		7
24	Power-on-reset circuit with power-off auto-discharging path for passive RFID tag ICs. , 2010, , .		7
25	A low power asynchronous DES. , 0, , .		6
26	Current-Division-Based Digital Frequency Tuning for Active RC Filters. Analog Integrated Circuits and Signal Processing, 2005, 45, 61-69.	0.9	6
27	A Low-power BitStream Controller for H.264/AVC Baseline Decoding. , 2006, , .		6
28	Low-Cost VC Allocator Design for Virtual Channel Wormhole Routers in Networks-on-Chip. , 2008, , .		6
29	A Low-power signal processing front-end and decoder for UHF passive RFID transponders. , 2009, , .		6
30	A 0.4 V low power baseband processor for UHF passive RFID tags. , 2010, , .		6
31	Clock recovery circuit with adiabatic technology (quasi-static CMOS logic). , 0, , .		5
32	Robust and low complexity packet detector design for MB-OFDM UWB. , 2009, , .		5
33	A self-timed divider using a new fast and robust pipeline scheme. IEEE Journal of Solid-State Circuits, 2001, 36, 917-923.	3.5	4
34	CMOS RF LNA with high ESD immunity. , 0, , .		4
35	A Speech Recognition IC Using Hidden Markov Models with Continuous Observation Densities. Journal of Signal Processing Systems, 2007, 47, 223-232.	1.0	4
36	Efficient and low complexity phase tracking method for MB-OFDM UWB receiver. , 2010, , .		4

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37	A 0.5ÂV 65.7ÂdB 1ÂMHz continuous-time complex delta sigma modulator. Analog Integrated Circuits and Signal Processing, 2011, 66, 255-267.	0.9	4
38	An asynchronous SOVA decoder for wireless communication application. , 0, , .		3
39	A 0.5V Fully Differential OTA with Local Common Feedback. , 0, , .		3
40	Power-efficient VLSI implementation of bitstream parsing in H.264/AVC decoder. , 0, , .		3
41	Power-Efficient VLSI Realization of a Complex FSM for H.264/AVC Bitstream Parsing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 984-988.	2.2	3
42	Power efficient and high speed frequency synchronizer design for MB-OFDM UWB. , 2009, , .		3
43	Subthreshold passive RF tag's PIE decoder design with wide tolerance and custom ratioed logic cells. , 2014, , .		3
44	Systolic array based VLSI architecture for high throughput 2-D discrete wavelet transform. , 2016, , .		3
45	A Subthreshold Baseband Processor Core Design With Custom Modules and Cells for Passive RFID Tags. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 159-167.	1.9	3
46	An useful micropipeline architecture to implement DSP algorithms. , 0, , .		2
47	A High-Efficiency Strongly Self-Checking Asynchronous Datapath. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 1484-1491.	1.9	2
48	0.8 V GPS band CMOS VCO with 29% Tuning Range. , 2006, , .		2
49	A 6-digit CMOS Current-Mode Analog-to-Quaternary Converter with RSD Error Correction Algorithm. , 0, , .		2
50	A fully differential low noise amplifier with real-time channel hopping for ultra-wideband wireless applications. , 0, , .		2
51	A network-on-Chip system-level simulation environment supporting asynchronous router. , 2007, , .		2
52	Low-Cost Allocator Implementations for Networks-on-Chip Routers. VLSI Design, 2009, 2009, 1-10.	0.5	2
53	A novel mismatch cancellation and I/Q channel multiplexing scheme for quadrature bandpass ΔΣ modulators. , 2009, , .		2
54	A simulation-oriented channel modeling methodology for human on-body channel communication. , 2012, , .		2

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55	Design a Low-Power H.264/AVC Baseline Decoder at All Abstraction Levelsâ€"A Showcase. Journal of Signal Processing Systems, 2012, 67, 317-330.	1.4	2
56	A 0.35 V 376 Mb/s Configurable Long Integer Multiplier for Subthreshold Encryption. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1430-1434.	2.2	2
57	A 12-bit 80 Ms/s 110 mW floating analog-to-digital converter. , 0, , .		1
58	Self-timed Booth's multiplier. , 0, , .		1
59	CMOS high speed interpolators based on parallel architecture. IEEE Transactions on Consumer Electronics, 2000, 46, 326-329.	3.0	1
60	A totally self-checking dynamic asynchronous datapath. , 0, , .		1
61	Design for self-checking and self-timed datapath. , 0, , .		1
62	A contactless smartcard designed with asynchronous circuit technique. , 0, , .		1
63	A new current mirror memory cell to improve the power efficiency of CMOS current mode analog circuits. , 0, , .		1
64	A Speech Recognizer With Selectable Model Parameters. , 0, , .		1
65	Active RC Filter with Reduced Capacitance by Current Division Technique. , 0, , .		1
66	A Sub-1 V 1.6 GHz CMOS VCO with 29% Tuning Range. , 2006, , .		1
67	A 6-digit RSD analog-to-quaternary converter with CMOS Current Mode Quaternary Adders. , 2007, , .		1
68	Design and challenges of passive UHF RFID tag in 90nm CMOS technology. , 2008, , .		1
69	A process-compatible passive RFID tag's digital design for subthreshold operation. , 2012, , .		1
70	A high-speed pipeline architecture of squarer-accumulator (SQAC). , 2016, , .		1
71	Subthreshold Passive RFID Tag's Baseband Processor Core Design with Custom Modules and Cells. , 2016, , .		1
72	Hardware acceleration of support vector machine based on high level synthesis. , 2018, , .		1

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73	A 0.4 V 298 nJ/op Neural Signal Spectral Feature Extraction Module With Novel Approximate MACs and Custom Compressors. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1733-1737.	2.2	1
74	A pipelined dataflow small micro-coded asynchronous processor and its application to DCT. , 0, , .		0
75	A 500 MHz digital-to-analog converter with curve interpolation. , 0, , .		0
76	A CMOS current feedback operational amplifier with active current mode compensation. , 0, , .		0
77	A 1 V 1.1 GHz CMOS integrated receiver front-end. , 0, , .		0
78	A low power asynchronous java processor for contactless smart card. , 0, , .		0
79	High Speed Curve Interpolating D/A Converter. Journal of Signal Processing Systems, 2004, 38, 5-11.	1.0	0
80	A sub-harmonic oscillator using an injection-locked DCO. , 0, , .		0
81	Ramp Voltage Supply using Adiabatic Charging Principle. , 0, , .		0
82	Realization of Card-Centric Framework: A Card-Centric Computer. , 0, , .		0
83	A 75dB image rejection IF-input quadrature sampling SC ΣΔ modulator. , 0, , .		0
84	An optimal normal basis elliptic curve cryptoprocessor for inductive RFID application. , 0, , .		0
85	Sub-1 V Current Mode CMOS Integrated Receiver Front-end for GPS System. , 2006, , .		0
86	Design challenges of voltage multiplier in a 0.35-μm 2-poly 4-metal CMOS technology for RFID passive tags. , 2007, , .		0
87	A passive RFID tag IC development platform. , 2009, , .		0
88	A quaternary current mode bus driver and receiver circuits. , 2009, , .		0
89	Performance evaluation of OFDM de-modulator with various multiplier architectures for UWB system. , 2010, , .		0
90	Robust and efficient baseband receiver design for MB-OFDM UWB system. , 2011, , .		0

#	Article	IF	Citations
91	Key component designs of subthreshold baseband processors in passive RF device. , 2013, , .		0
92	Ultra-low-power robust and compatible digital IPs for passive RF devices. , 2013, , .		0
93	A novel ratioed logic style for faster subthreshold digital circuits based on 90 nm CMOS and below. , 2014, , .		0
94	Subthreshold passive RFID tag's baseband processor core design with custom modules and cells. , 2015, , .		0
95	Reduced complexity look-up table based Ï€-rotation LDPC decoder. , 2016, , .		0
96	A 0.4V 320Mb/s 28.7ÂµW 1024-bit configurable multiplier for subthreshold SOC encryption. , 2016, , .		0
97	23 ÂµW 8.9â€effective number of bit 1.1ÂMS/s successive approximation register analogâ€toâ€digital converter with an energyâ€efficient digitalâ€toâ€analog converter switching scheme. Journal of Engineering, 2014, 2014, 420-425.	0.6	0