Nobutaka Kuroki

List of Publications by Year
in descending order

64 papers	825 citations	1307594 7 h-index	677142 22 g-index
64 all docs	64 docs citations	64 times ranked	521 citing authors

#	Article	IF	Citations
1	1.2-V Supply, 100-nW, 1.09-V Bandgap and 0.7-V Supply, 52.5-nW, 0.55-V Subbandgap Reference Circuits for Nanowatt CMOS LSIs. IEEE Journal of Solid-State Circuits, 2013, 48, 1530-1538.	5.4	215
2	A Low-Power Level Shifter With Logic Error Correction for Extremely Low-Voltage Digital CMOS LSIs. IEEE Journal of Solid-State Circuits, 2012, 47, 1776-1783.	5.4	94
3	A nano-ampere current reference circuit and its temperature dependence control by using temperature characteristics of carrier mobilities. , 2010, , .		73
4	Fully-Integrated High-Conversion-Ratio Dual-Output Voltage Boost Converter With MPPT for Low-Voltage Energy Harvesting. IEEE Journal of Solid-State Circuits, 2016, 51, 2398-2407.	5.4	61
5	A CMOS bandgap and sub-bandgap voltage reference circuits for nanowatt power LSIs. , 2010, , .		36
6	An 80-mV-to-1.8-V Conversion-Range Low-Energy Level Shifter for Extremely Low-Voltage VLSIs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2026-2035.	5.4	34
7	A 32.55-kHz, 472-nW, 120ppm/°C, fully on-chip, variation tolerant CMOS relaxation oscillator for a real-time clock application. , 2013, , .		29
8	A 0.19-V minimum input low energy level shifter for extremely low-voltage VLSIs. , 2015, , .		21
9	A 0.21-V minimum input, 73.6% maximum efficiency, fully integrated voltage boost converter with MPPT for low-voltage energy harvesters. , 2014, , .		18
10	A 0.1–0.6 V input range voltage boost converter with low-leakage driver for low-voltage energy harvesting. , 2017, , .		18
11	A Highly Efficient Switched-Capacitor Voltage Boost Converter with Nano-Watt MPPT Controller for Low-Voltage Energy Harvesting. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2016, E99.A, 2491-2499.	0.3	14
12	A 18.9-nA standby current comparator with adaptive bias current generator. , 2011, , .		11
13	A nano-watt power CMOS amplifier with adaptive biasing for power-aware analog LSIs. , 2012, , .		11
14	A 6.66-kHz, 940-nW, 56ppm/°C, fully on-chip PVT variation tolerant CMOS relaxation oscillator. , 2012, , .		10
15	A 0.38-µW stand-by power, 50-nA-to-1-mA load current range DC-DC converter with self-biased linear regulator for ultra-low power battery management. , 2016, , .		10
16	Nano-ampere CMOS current reference with little temperature dependence using small offset voltage. , 2010, , .		9
17	A low-power single-slope analog-to-digital converter with digital PVT calibration. , 2012, , .		8
18	Delay-compensation techniques for ultra-low-power subthreshold CMOS digital LSIs. , 2009, , .		7

#	Article	IF	Citations
19	A level shifter with logic error correction circuit for extremely low-voltage digital CMOS LSIs. , 2011, , .		7
20	Ultralow-quiescent-current and wide-load-range low-dropout linear regulator with self-biasing technique for micropower battery management. Japanese Journal of Applied Physics, 2017, 56, 04CF11.	1.5	7
21	Multi-Channel Convolutional Neural Networks for Image Super-Resolution. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2017, E100.A, 572-580.	0.3	7
22	Switched-Capacitor Voltage Buck Converter with Step-Down-Ratio and Clock-Frequency Controllers for Ultra-Low-Power IoT Devices. , 2018, , .		7
23	Automated Fish Bone Detection in Xâ€Ray Images with Convolutional NeuralÂNetwork and Synthetic Image Generation. IEEJ Transactions on Electrical and Electronic Engineering, 2021, 16, 1510-1517.	1.4	7
24	A level shifter circuit design by using input/output voltage monitoring technique for ultra-low voltage digital CMOS LSIs. , 2011, , .		6
25	A fully-integrated, high-conversion-ratio and dual-output voltage boost converter with MPPT for low-voltage energy harvesting. , 2015, , .		6
26	Impedance matching in magnetic-coupling-resonance wireless power transfer for small implantable devices. , 2017, , .		6
27	A 0.21-V minimum input, 73.6% maximum efficiency, fully integrated 3-terminal voltage converter with MPPT for low-voltage energy harvesters. , 2015, , .		5
28	Image super-resolution with multi-channel convolutional neural networks. , 2016, , .		5
29	Detecting tampered regions in JPEG images via CNN. , 2020, , .		5
30	A 35-mV supply ring oscillator consisting of stacked body bias inverters for extremely low-voltage LSIs. IEICE Electronics Express, 2021, 18, 20210065-20210065.	0.8	5
31	A wide input voltage range level shifter circuit for extremely low-voltage digital LSIs. IEICE Electronics Express, 2011, 8, 890-896.	0.8	4
32	An ultra-low-power supercapacitor voltage monitoring system for low-voltage energy harvesting. , 2017, , .		4
33	An ultra-low power active diode using a hysteresis common gate comparator for low-voltage and low-power energy harvesting systems. , 2018, , .		4
34	Analytical Study of Multi-stage Switched-Capacitor Voltage Boost Converter for Ultra-low Voltage Energy Harvesting. , 2018, , .		4
35	Sub-0.1V Input, Low-Voltage CMOS Driver Circuit for Multi-Stage Switched Capacitor Voltage Boost Converter. , 2019, , .		4
36	Combination of Convolutional Neural Network Architecture and its Learning Method for Rotationâ€Invariant Handwritten Digit Recognition. IEEJ Transactions on Electrical and Electronic Engineering, 2021, 16, 161-163.	1.4	4

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37	Multi-Category Image Super-Resolution with Convolutional Neural Network and Multi-Task Learning. IEICE Transactions on Information and Systems, 2021, E104.D, 183-193.	0.7	4
38	Detecting Doctored JPEG Image Based on Block Noise Analysis and Double JPEG Analysis. IEEJ Transactions on Electronics, Information and Systems, 2017, 137, 742-749.	0.2	4
39	Super-resolution technique for thermography with dual-camera system. , 2010, , .		3
40	A 95-nA, 523ppm/°C, 0.6-μW CMOS current reference circuit with subthreshold MOS resistor ladder. , 2011, , .		3
41	High current efficiency sense amplifier using body-bias control for ultra-low-voltage SRAM. , 2011, , .		3
42	A 24-transistor static flip-flop consisting of nors and inverters for low-power digital vlsis. , 2014, , .		3
43	Energy-efficient AES SubBytes transformation circuit using asynchronous circuits for ultra-low voltage operation. IEICE Electronics Express, 2015, 12, 20141157-20141157.	0.8	3
44	A 34-mV Startup Ring Oscillator Using Stacked Body Bias Inverters for Extremely Low-Voltage Thermoelectric Energy Harvesting. , 2020, , .		3
45	An 11.8 nA ultra-low power active diode using a hysteresis common gate comparator for low-power energy harvesting systems. IEICE Electronics Express, 2020, 17, 20200103-20200103.	0.8	3
46	An Area-Efficient Resistor-less On-Chip Frequency Reference for Ultra-Low Power Real-Time Clock Application. IEEJ Transactions on Electrical and Electronic Engineering, 2018, 13, 1633-1641.	1.4	2
47	Subthreshold SRAM with Write Assist Technique Using On-Chip Threshold Voltage Monitoring Circuit. IEICE Transactions on Electronics, 2011, E94-C, 1042-1048.	0.6	2
48	An Energy-Efficient 24T Flip-Flop Consisting of Standard CMOS Gates for Ultra-Low Power Digital VLSIs. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2015, E98.A, 2600-2606.	0.3	2
49	Locally Weighted Averaging for Denoising of Medical Tomographic Images. Journal of Signal Processing, 2016, 20, 217-220.	0.3	2
50	A Sub-1-Âµs Start-Up Time, Fully-Integrated 32-MHz Relaxation Oscillator for Low-Power Intermittent Systems. IEICE Transactions on Electronics, 2018, E101.C, 161-169.	0.6	2
51	Detecting Doctored Region in JPEG Image using Convolutional Neural Networks. IEEJ Transactions on Electronics, Information and Systems, 2018, 138, 1417-1424.	0.2	2
52	Haar wavelet transform with interband prediction and its application to image coding. Electronics and Communications in Japan, Part III: Fundamental Electronic Science (English Translation of Denshi) Tj ETQq0 0 0rgBT /Overlock 10 Tf		1
53	Layered blind deconvolution with interband prediction. Systems and Computers in Japan, 2000, 31, 77-83.	0.2	1
54	Switching-voltage detection and compensation circuits for ultra-low-voltage CMOS inverters. , 2009, , .		1

#	ARTICLE	IF	CITATIONS
55	A 105-nW CMOS thermal sensor for power-aware applications. , 2011, , .		1
56	Robust Subthreshold CMOS Digital Circuit Design with On-Chip Adaptive Supply Voltage Scaling Technique. IEICE Transactions on Electronics, 2011, E94-C, 80-88.	0.6	1
57	Super-Resolution with Multi-Path Convolutional Neural Networks. IEEJ Transactions on Electronics, Information and Systems, 2020, 140, 638-650.	0.2	1
58	Improvement of Luminance Isotropy for Convolutional Neural Networks-Based Image Super-Resolution. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2020, E103.A, 955-958.	0.3	1
59	Detecting tampered region in video using LSTM and U‑Net. Electronics and Communications in Japan, 2020, 103, 15-25.	0.5	1
60	Write-assisted subthreshold SRAM by using on-chip threshold voltage monitoring circuit. , 2010, , .		0
61	An Error Diagnosis Technique Based on Location Sets to Rectify Subcircuits. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 3136-3142.	0.3	0
62	An Error Diagnosis Technique Based on Clustering of Elements. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2010, E93-A, 2490-2496.	0.3	0
63	Super-Resolution with Horizontal and Vertical Convolutional Neural Networks. IEEJ Transactions on Electronics, Information and Systems, 2018, 138, 957-963.	0.2	0
64	Detecting Tampered Region in video using LSTM and U-Net. IEEJ Transactions on Electronics, Information and Systems, 2020, 140, 476-483.	0.2	0