Omid Shoaei

List of Publications by Year
in descending order

76	402	1040056	888059
papers	citations	9	17
		h-index	g-index

77	77	77	360
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Fast Background Calibration of Linear and Non-Linear Errors in Pipeline Analog-to-Digital Converters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 884-888.	3.0	3
2	Current-Based Neurostimulation Circuit and System Techniques. , 2022, , 445-469.		1
3	A Class-E Power and Data Transmitter With Improved Data Rate to Carrier Frequency Ratio for Medical Implants. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2692-2696.	3.0	0
4	A Low-Complexity and High-Resolution Beamformer for Portable Medical Ultrasound Imaging. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 2022, 69, 2226-2235.	3.0	0
5	A 7.2ÂµW Magnitude/Phase Bio-impedance Measurement Front-End with PWM Output in 0.18Âµm CMOS. , 2021, , .		0
6	An asynchronous pulse width modulator for DCâ€ĐC buck converter. International Journal of Circuit Theory and Applications, 2020, 48, 231-253.	2.0	3
7	A buck converter based on dual mode asynchronous pulse width modulator. AEU - International Journal of Electronics and Communications, 2020, 114, 152998.	2.9	2
8	Analysis and design of an asynchronous pulseâ€width modulation technique for switch mode power supply. IET Power Electronics, 2020, 13, 1639-1648.	2.1	2
9	A high efficient adiabatic Transcutaneous Electrical Nerve Stimulator (TENS) with current regulation. AEU - International Journal of Electronics and Communications, 2020, 123, 153275.	2.9	4
10	A 9-Bit 70-MS/s Two-Stage SAR ADC With Passive Residue Transfer. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1185-1194.	3.1	4
11	Current-Based Neurostimulation Circuit and System Techniques. , 2020, , 1-26.		0
12	A comprehensive circuit model for evaluating the response of silicon photomultipliers in continuous wave light regime. International Journal of Circuit Theory and Applications, 2019, 47, 1585-1602.	2.0	0
13	Performance Evaluation of Silicon Photomultipliers for Frequency-Domain Fluorescence Lifetime Measurement Based on a Comprehensive Circuit Model. IEEE Journal of Quantum Electronics, 2019, 55, 1-9.	1.9	0
14	Modified linear in dB, sub 0.2ÂdB gain-step CMOS programmable gain amplifier for ultrasound applications. Analog Integrated Circuits and Signal Processing, 2019, 99, 497-508.	1.4	2
15	A Reconfigurable Dual-Mode Tracking SAR ADC without Analog Subtraction. , 2019, , .		1
16	A power efficient, differential multichannel adiabatic electrode stimulator for deep brain stimulation. Analog Integrated Circuits and Signal Processing, 2018, 95, 481-497.	1.4	4
17	A 0.5â€Î¼A/Channel front-end for implantable and external ambulatory ECG recorders. Microelectronics Journal, 2018, 74, 79-85.	2.0	10
18	Enhanced Power-Delivered-to-Load Through Planar Multiple-Harmonic Wireless Power Transmission. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1219-1223.	3.0	17

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19	A 1.55 Î¼W Bio-Impedance Measurement System for Implantable Cardiac Pacemakers in 0.18 Î¼m CMOS. IEEE Transactions on Biomedical Circuits and Systems, 2018, 12, 211-221.	4.0	37
20	A 0.36ÂÎ¼W/channel recorder for external ambulatory ECG recorders. Analog Integrated Circuits and Signal Processing, 2018, 95, 17-29.	1.4	1
21	ADC-Assisted Random Sampler Architecture for Efficient Sparse Signal Acquisition. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1590-1594.	3.1	2
22	Improved Wireless Power Transfer Efficiency Using Reactively Terminated Resonators. IEEE Antennas and Wireless Propagation Letters, 2018, 17, 803-807.	4.0	7
23	Distributedâ€element modelling for spiral resonators used in wireless power transfer. International Journal of Circuit Theory and Applications, 2018, 46, 313-327.	2.0	3
24	Mixed-Signal IC With Pulse Width Modulation Wireless Telemetry for Implantable Cardiac Pacemakers in 0.18-Î¼m CMOS. IEEE Transactions on Biomedical Circuits and Systems, 2018, 12, 1-12.	4.0	14
25	Design, Analysis, Simulation, and Fabrication of a Novel Linear MEMS Capacitive Inclinometer. IEEE Sensors Journal, 2018, 18, 6962-6968.	4.7	3
26	Statistical estimation of delay in nano-scale CMOS circuits using Burr Distribution. Microelectronics Journal, 2018, 79, 30-37.	2.0	7
27	A Fully Fail-Safe Capacitive-Based Charge Metering Method for Active Charge Balancing in Deep Brain Stimulation. , 2018, , .		4
28	Capacitive cancellation technique in design of CMOS low noise amplifier for ultrasound applications. Analog Integrated Circuits and Signal Processing, 2017, 91, 163-169.	1.4	0
29	Linear in dB, sub 0.2ÂdB gain-step CMOS programmable gain amplifier for ultrasound applications. Analog Integrated Circuits and Signal Processing, 2017, 93, 309-318.	1.4	4
30	Effective method for knock signal denoising in internal combustion engine. International Journal of Automotive Technology, 2017, 18, 769-777.	1.4	4
31	An aging-aware model for the leakage power of nanoscaled digital integrated circuits in IoT era. , 2017, , .		1
32	Knock signal denoising employing a new time domain method. , 2017, , .		1
33	Two-electrode impedance-sensing cardiac rhythm monitor for charge-aware shock delivery in cardiac arrest. , 2017, , .		2
34	A wireless pulsed-current battery charger for implantable biomedical stimulators. , 2016, , .		5
35	Extended coupling-range wireless power transfer using 0Ã— / 4Ã— resonant regulating rectifier. , 2016, , .		0
36	A Power optimized switched-capacitor based approach in voltage-controlled cardiac stimulation. , 2016, , .		0

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37	A CMOS pseudo-exponential current-output DAC with code-dependent body-biasing. Analog Integrated Circuits and Signal Processing, 2016, 88, 127-136.	1.4	1
38	A high power efficient multi-waveform current stimulator used in implantable neural stimulation. Analog Integrated Circuits and Signal Processing, 2016, 86, 459-469.	1.4	6
39	A low-power digitally closed-loop electrical stimulator suited for low-pulse-width-stimulation. , 2015, , .		1
40	A simple and precise charge balancing method for voltage mode stimulation. , 2014, , .		14
41	A passive implantable biopotential measurement sensor with an inductive coupled readout circuit. , 2014, , .		0
42	Polarity detection base pulse insertion for active charge balancing in electrical stimulation. , 2014, , .		4
43	High speed sample and hold design using closed-loop pole-zero cancelation. Microelectronics Journal, 2011, 42, 1353-1358.	2.0	4
44	Linearity improvement of open-loop NMOS source-follower sample and hold circuits. IET Circuits, Devices and Systems, 2011, 5, 1.	1.4	9
45	IIP2 Improvement Techniques for Multi-standard Mobile Radio. Integrated Circuits and Systems, 2009, , 169-202.	0.2	0
46	A Novel Low Power 1 GS/s S&H Architecture With Improved Analog Bandwidth. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 971-975.	3.0	4
47	A High IIP2 Mixer Enhanced by a New Calibration Technique for Zero-IF Receivers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 219-223.	3.0	29
48	A 0.9V 10-bit 100 MS/s switched-RC pipelined ADC without using a front-end S/H in 90nm CMOS. , 2008, , .		3
49	A high dynamic range multi-standard CMOS mixer for GSM, UMTS and IEEE802.11b-g-a applications. , 2008, , .		5
50	New technique in design of active rf cmos mixers for low flicker noise and high conversion gain. , 2008, , .		1
51	A low-voltage low-power highly-linear switched-RC MDAC for pipelined ADCs. IEICE Electronics Express, 2008, 5, 67-73.	0.8	1
52	A new reconfigurable LNA enhanced by programmable load and capacitive feedback for multi-standard applications. IEICE Electronics Express, 2007, 4, 159-164.	0.8	3
53	500MSPS with 80dB SFDR SHA for Time interleaved application using LATERAL PNP in CMOS process. , 2007, , .		0
54	A Low Power Fast Settling CMOS S&H utilizing Auxiliary Slew Circuits. , 2007, , .		0

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55	A 0.9-V 10-bit 100-MSample/s pipelined ADC using switched-RC and opamp sharing techniques. Midwest Symposium on Circuits and Systems, 2007, , .	1.0	1
56	A New IIP2 Enhancement Technique for CMOS Down-Converter Mixers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 1062-1066.	3.0	13
57	Experimental Evaluation of Different Realizations of Recursive CIC Filters. , 2006, , .		2
58	A High Speed and Power Controlled CMOS Edge Detector for 2.5 Gb/s Clock Recovery Circuit. , 2006, , .		0
59	Continuous Time Delta-Sigma Modulators with Arbitrary DAC Waveforms. , 2006, , .		3
60	A New Approach for DAC Non-linearity Compensation in Continuous Time Delta Sigma Modulators. , 2006, , .		0
61	Implementation of Multiplier Block with Reduced Adder Cost. , 2006, , .		1
62	A 0.18μm, 1.8-V CMOS High Gain Fully Differential Opamp Utilized in Pipelined ADC. , 2006, , .		2
63	Design of High-Precision Low-Power Interpolation Modules with Modified SINC Filters. , 2006, , .		1
64	A Straightforward Design Methodology for Multi-bit Continuous Time Delta Sigma Modulators. Midwest Symposium on Circuits and Systems, 2006, , .	1.0	3
65	A complete analysis of noise in inductively source degenerated CMOS LNA's. IEICE Electronics Express, 2005, 2, 25-31.	0.8	3
66	Efficient double-sampled cascaded .SIGMA..DELTA. modulator topologies for low OSRs. IEICE Electronics Express, 2005, 2, 404-410.	0.8	0
67	A novel fully-differential class AB folded-cascode OTA for switched-capacitor applications. , 2005, , .		3
68	Modeling of Switched-Capacitor Deltaâ€“Sigma Modulators in SIMULINK. IEEE Transactions on Instrumentation and Measurement, 2005, 54, 1646-1654.	4.7	74
69	Multiply-by-two gain stage with reduced mismatch sensitivity. Electronics Letters, 2005, 41, 289.	1.0	12
70	Systematic design of the pipelined analog-to-digital converter with radix<2. Microelectronics Journal, 2004, 35, 767-776.	2.0	2
71	A novel fully-differential class AB folded-cascode OTA. IEICE Electronics Express, 2004, 1, 358-362.	0.8	3
72	Return to-zero feedback insertion in a continuous time Delta-Sigma modulator for excess loop delay compensation. IEICE Electronics Express, 2004, 1, 568-574.	0.8	5

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73	Title is missing!. Analog Integrated Circuits and Signal Processing, 2003, 37, 149-163.	1.4	3
74	Low-power design techniques for low-voltage fast-settling operational amplifiers in switched-capacitor applications. The Integration VLSI Journal, 2003, 36, 175-189.	2.1	20
75	Low-voltage low-power fast-settling CMOS operational transconductance amplifiers for switched-capacitor applications. , 2003, , .		8
76	Very low-voltage, low-power and fast-settling OTA for switched-capacitor applications. , 0, , .		10