Linda Milor

List of Publications by Year
in descending order

105	694	687220 13	887953 17
papers	citations	h-index	g-index

106	106	106	274
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Reliable cache design with on-chip monitoring of NBTI degradation in SRAM cells using BIST. , 2010, , .		39
2	System-level variation-aware aging simulator using a unified novel gate-delay model for bias temperature instability, hot carrier injection, and gate oxide breakdown. Microelectronics Reliability, 2015, 55, 1334-1340.	0.9	25
3	System-Level Modeling and Microprocessor Reliability Analysis for Backend Wearout Mechanisms. , 2013, , .		22
4	Methodology to determine the impact of linewidth variation on chip scale copper/low-k backend dielectric breakdown. Microelectronics Reliability, 2010, 50, 1341-1346.	0.9	21
5	A Survey of Yield Modeling and Yield Enhancement Methods. IEEE Transactions on Semiconductor Manufacturing, 2013, 26, 196-213.	1.4	21
6	System-level modeling of microprocessor reliability degradation due to BTI and HCI. , 2014, , .		21
7	Backend low-k TDDB chip reliability simulator. , 2011, , .		20
8	Microprocessor Aging Analysis and Reliability Modeling Due to Back-End Wearout Mechanisms. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2065-2076.	2.1	18
9	SRAM stability analysis for different cache configurations due to Bias Temperature Instability and Hot Carrier Injection. , 2016, , .		18
10	Towards a chip level reliability simulator for copper/low-k backend processes. , 2010, , .		17
11	NBTI resistant SRAM design. , 2011, , .		17
12	Online Measurement of Degradation Due to Bias Temperature Instability in SRAMs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2184-2194.	2.1	17
13	System-Level Modeling of Microprocessor Reliability Degradation Due to Bias Temperature Instability and Hot Carrier Injection. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2712-2725.	2.1	17
14	A methodology to extract failure rates for low-k dielectric breakdown with multiple geometries and in the presence of die-to-die linewidth variation. Microelectronics Reliability, 2009, 49, 1096-1102.	0.9	15
15	Area Scaling for Backend Dielectric Breakdown. IEEE Transactions on Semiconductor Manufacturing, 2010, 23, 429-441.	1.4	15
16	Analysis and On-Chip Monitoring of Gate Oxide Breakdown in SRAM Cells. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 855-864.	2.1	15
17	Comprehensive reliability and aging analysis on SRAMs within microprocessor systems. Microelectronics Reliability, 2015, 55, 1290-1296.	0.9	15
18	Comprehensive Reliability-Aware Statistical Timing Analysis Using a Unified Gate-Delay Model for Microprocessors. IEEE Transactions on Emerging Topics in Computing, 2018, 6, 219-232.	3.2	15

#	Article	IF	Citations
19	Modeling Low-k Dielectric Breakdown to Determine Lifetime Requirements. IEEE Design and Test of Computers, 2009, 26, 18-27.	1.4	14
20	A Comprehensive Time-Dependent Dielectric Breakdown Lifetime Simulator for Both Traditional CMOS and FinFET Technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2470-2482.	2.1	14
21	A DLL Design for Testing I/O Setup and Hold Times. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1579-1592.	2.1	13
22	System-level modeling and reliability analysis of microprocessor systems. , 2013, , .		13
23	Backend dielectric chip reliability simulator for complex interconnect geometries. , 2012, , .		11
24	Accurate standard cell characterization and statistical timing analysis using multivariate adaptive regression splines. , 2015, , .		10
25	Built-In Self-Test Methodology With Statistical Analysis for Electrical Diagnosis of Wearout in a Static Random Access Memory Array. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2521-2534.	2.1	10
26	Study of Area Scaling Effect on Integrated Circuit Reliability Based on Yield Models. Microelectronics Reliability, 2005, 45, 1305-1310.	0.9	9
27	Backend dielectric breakdown dependence on linewidth and pattern density. Microelectronics Reliability, 2007, 47, 1473-1477.	0.9	9
28	Analysis of the impact of linewidth variation on low-k dielectric breakdown. , 2010, , .		9
29	Front-end of line and middle-of-line time-dependent dielectric breakdown reliability simulator for logic circuits. Microelectronics Reliability, 2017, 76-77, 81-86.	0.9	9
30	A comparative study of wearout mechanisms in state-of-art microprocessors. , 2012, , .		8
31	Processor-level reliability simulator for time-dependent gate dielectric breakdown. Microprocessors and Microsystems, 2015, 39, 950-960.	1.8	8
32	Impact of NBTI/PBTIon SRAMs within microprocessor systems: Modeling, simulation, and analysis. Microelectronics Reliability, 2013, 53, 1183-1188.	0.9	7
33	Backend Dielectric Reliability Full Chip Simulator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1750-1762.	2.1	7
34	Analysis of time-dependent dielectric breakdown induced aging of SRAM cache with different configurations. Microelectronics Reliability, 2017, 76-77, 87-91.	0.9	7
35	SRAM Stability Analysis and Performanceâ€“Reliability Tradeoff for Different Cache Configurations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 620-633.	2.1	7
36	Modeling of the breakdown mechanisms for porous copper/low-k process flows. Microelectronics Reliability, 2007, 47, 1478-1482.	0.9	6

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37	Built-in self test methodology for diagnosis of backend wearout mechanisms in SRAM cells. , 2014, , .		6
38	Impact of stress acceleration on mixed-signal gate oxide lifetime. , 2015, , .		6
39	Negative Bias Temperature Instability and Gate Oxide Breakdown Modeling in Circuits With Die-to-Die Calibration Through Power Supply and Ground Signal Measurements. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2271-2284.	2.1	6
40	Circuit-level reliability simulator for front-end-of-line and middle-of-line time-dependent dielectric breakdown in FinFET technology. , 2018, , .		6
41	Modeling of FinFET SRAM array reliability degradation due to electromigration. Microelectronics Reliability, 2019, 100-101, 113485.	0.9	6
42	Modeling of defect propagation/growth for yield impact prediction in VLSI manufacturing. Proceedings of SPIE, 1997, , .	0.8	5
43	Determining the Impact of Within-Die Variation on Circuit Timing. IEEE Transactions on Semiconductor Manufacturing, 2011, 24, 385-391.	1.4	5
44	An ECC-Assisted Postpackage Repair Methodology in Main Memory Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2045-2058.	2.1	5
45	Modeling for SRAM reliability degradation due to gate oxide breakdown with a compact current model. , 2017, , .		5
46	Modeling of the reliability degradation of a FinFET-based SRAM due to bias temperature instability, hot carrier injection, and gate oxide breakdown. , 2017, , .		5
47	Optimization of Experimental Designs for System- Level Accelerated Life Test in a Memory System Degraded by Time-Dependent Dielectric Breakdown. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1640-1651.	2.1	5
48	Impact of front-end wearout mechanisms on FinFET SRAM soft error rate. Microelectronics Reliability, 2019, 100-101, 113487.	0.9	5
49	Impact of CD control on circuit yield in submicron lithography. , 1992, 1671, 357.		4
50	Ring oscillator based embedded structure for decoupling PMOS/NMOS degradation with switching activity replication. , 2010, , .		4
51	Wearout-aware compiler-directed register assignment for embedded systems. , 2012, , .		4
52	Backend dielectric reliability simulator for microprocessor system. Microelectronics Reliability, 2012, 52, 1953-1959.	0.9	4
53	Diagnosis of resistive-open defects due to electromigration and stress-induced voiding in an SRAM array. , 2014, , .		4
54	Memory BIST for on-chip monitoring of resistive-open defects due to electromigration and stress-induced voiding in an SRAM array. , 2014, , .		4

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55	Simulation of system backend dielectric reliability. Microelectronics Journal, 2014, 45, 1327-1334.	1.1	4
56	Machine Learning for Detection of Competing Wearout Mechanisms. , 2019, , .		4
57	Diagnosis of Optical Lithography Faults With Product Test Sets. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1657-1669.	1.9	3
58	A BIST Circuit for DLL Fault Detection. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 1687-1695.	2.1	3
59	Reliable cache design with detection of gate oxide breakdown using BIST. , 2009, , .		3
60	Via wearout detection with on chip monitors. , 2009, , .		3
61	Gate oxide breakdown parameter extraction with ground and power supply signature measurements. , 2014, , .		3
62	Estimation of remaining life using embedded SRAM for wearout parameter extraction. , 2015, , .		3
63	TDDB-emerald: A methodology for estimating memory reliability degradation resulting from time-dependent dielectric breakdown. , 2016, , .		3
64	A comparison study of time-dependent dielectric breakdown for analog and digital circuit's optimal accelerated test regions. , 2017, , .		3
65	A lifetime and power sensitive design optimization framework for a radio frequency circuit. , 2017, , .		3
66	Estimation of the Optimal Accelerated Test Region for FinFET SRAMs Degraded by Front-End and Back-End Wearout Mechanisms. , 2018, , .		3
67	Impact of Front-End Wearout Mechanisms on the Performance of a Ring Oscillator-Based Thermal Sensor. , 2019, , .		3
68	A Comprehensive Framework for Analysis of Time-Dependent Performance-Reliability Degradation of SRAM Cache Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 857-870.	2.1	3
69	Characterization of spatial CD variability, spatial mask-level correction, and improvement of circuit performance. , 2000, , .		2
70	Porosity-Induced Electric Field Enhancement and Its Impact on Charge Transport in Porous Inter-Metal Dielectrics. , 2006, , .		2
71	Timing Analysis with Compact Variation-Aware Standard Cell Models. , 2009, , .		2
72	Via wearout detection with on-chip monitors. Microelectronics Journal, 2010, 41, 789-800.	1.1	2

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73	Impact of die partitioning on reliability and yield of 3D DRAM. , 2014, , .		2
74	Impact of Linewidth on Backend Dielectric TDDB and Incorporation of the Linewidth Effect in Full Chip Lifetime Analysis. IEEE Transactions on Semiconductor Manufacturing, 2015, 28, 25-34.	1.4	2
75	MBIST and statistical hypothesis test for time dependent dielectric breakdowns due to GOBD vs. BTDDB in an SRAM array. , 2015, , .		2
76	Analysis of errors in estimating wearout characteristics of time-dependent dielectric breakdown using system-level accelerated life test. Microelectronics Reliability, 2017, 76-77, 47-52.	0.9	2
77	Memory reliability estimation degraded by TDDB using circuit-level accelerated life test. , 2017, , .		2
78	Optimal Accelerated Test Regions for Time- Dependent Dielectric Breakdown Lifetime Parameters Estimation in FinFET Technology. , 2018, , .		2
79	A library based on deep neural networks for modeling the degradation of FinFET SRAM performance metrics due to aging. Microelectronics Reliability, 2019, 100-101, 113486.	0.9	2
80	Optimal Accelerated Test Framework for Time-Dependent Dielectric Breakdown Lifetime Parameter Estimation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2658-2671.	2.1	2
81	Proximity effect correction for clock-rate maximization. , 1998, 3510, 82.		1
82	Timing analysis with compact variation-aware standard cell models. The Integration VLSI Journal, 2009, 42, 312-320.	1.3	1
83	Determination of the impact of field enhancement in low-k dielectric breakdown. , 2009, , .		1
84	Fast Variation-Aware Statistical Dynamic Timing Analysis. , 2009, , .		1
85	TDDB chip reliability in copper interconnects. , 2010, , .		1
86	Impact of irregular geometries on low-k dielectric breakdown. Microelectronics Reliability, 2011, 51, 1582-1586.	0.9	1
87	System-level modeling of microprocessor reliability degradation due to TDDB. , 2014, , .		1
88	Design for reliability: A duty-cycle management system for timing violations. , 2016, , .		1
89	A methodology for estimating memory lifetime using a system-level accelerated life test and error-correcting codes. , 2017, , .		1
90	On-line monitoring of system health using on-chip SRAMs as a wearout sensor. , 2017, , .		1

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91	Lifetime Estimation Using Ring Oscillators for Prediction in FinFET Technology. , 2018, , .		1
92	Reliability and Aging Analysis on SRAMs Within Microprocessor Systems. , 2018, , .		1
93	Reliability and Accelerated Testing of 14nm FinFET Ring Oscillators. , 2019, , .		1
94	Identification of Failure Modes for Circuit Samples with Confounded Causes of Failure. , 2019, , .		1
95	Inverse Design of FinFET SRAM Cells. , 2020, , .		1
96	Extraction of wearout model parameters using on-line test of an SRAM. Microelectronics Reliability, 2020, 114, 113756.	0.9	1
97	Application of rigorous topography simulation for modeling of defect propagation/growth in VLSI fabrication. , 1997, , .		0
98	BIST for testing of delay. , 2007, , .		0
99	On chip monitoring of via degradation. , 2009, , .		0
100	Impact of NBTI on analog components. , 2012, , .		0
101	Panel: Analog/RF BIST: Are we there yet?. , 2015, , .		0
102	Adaptive supply voltage and duty cycle controller for yield-power optimization of ICs. , 2017, , .		0
103	New Electromigration Model and Its Potential Application on Degradation Simulation for FinFET SRAM. , 2018, , .		0
104	Optimal sampling for accelerated testing in 14Ânm FinFET ring oscillators. Microelectronics Reliability, 2020, 114, 113753.	0.9	0
105	A Delay Evaluation Circuit for Analog BIST Function. IEICE Transactions on Electronics, 2013, E96.C, 393-401.	0.3	0