

Paula Lopez Martinez

List of Publications by Year in Descending Order

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

52
papers

237
citations

8
h-index

13
g-index

68
ext. papers

318
ext. citations

3.1
avg, IF

3.16
L-index

#	Paper	IF	Citations
52	0.6-V- I_{IN} 7.0-nA- I_{Q} 0.75-mA- I_{L} CMOS Capacitor-Less LDO for Low-Voltage Micro-Energy-Harvested Supplies. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2021 , 1-10	3.9	1
51	An 11 mA Capacitor-Less LDO with 3.08 nA Quiescent Current and SSF-Based Adaptive Biasing. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2021 , 1-1	3.5	0
50	1.88 nA Quiescent Current Capacitor-Less LDO with Adaptive Biasing Based on a SSF Absolute Voltage Difference Meter 2020 ,		3
49	On-Chip Solar Energy Harvester and PMU With Cold Start-Up and Regulated Output Voltage for Biomedical Applications. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2020 , 67, 1103-1114	3.9	7
48	On-Chip Solar Cell and PMU on the Same Substrate with Cold Start-Up from nW and 80 dB of Input Power Range for Biomedical Applications 2019 ,		2
47	Deep Learning-Based Multiple Object Visual Tracking on Embedded System for IoT and Mobile Edge Computing Applications. <i>IEEE Internet of Things Journal</i> , 2019 , 6, 5423-5431	10.7	47
46	Ultralow power voltage reference circuit for implantable devices in standard CMOS technology. <i>International Journal of Circuit Theory and Applications</i> , 2019 , 47, 991-1005	2	1
45	Corrections to Wireless Sensor Network With Perpetual Motes for Terrestrial Snail Activity Monitoring <i>IEEE Sensors Journal</i> , 2019 , 19, 6553-6553	4	
44	Micro-Energy Harvesting System Including a PMU and a Solar Cell on the Same Substrate With Cold Startup From 2.38 nW and Input Power Range up to 10 μ W Using Continuous MPPT. <i>IEEE Transactions on Power Electronics</i> , 2019 , 34, 5105-5116	7.2	14
43	In-pixel analog memories for a pixel-based background subtraction algorithm on CMOS vision sensors. <i>International Journal of Circuit Theory and Applications</i> , 2018 , 46, 1631	2	2
42	Pulsed time-of-flight pixel with on-chip 20 μ klux background light suppression in standard CMOS technology. <i>International Journal of Circuit Theory and Applications</i> , 2018 , 46, 987-1005	2	
41	Effect of temporal and spatial noise on the performance of hardware oriented background extraction algorithms 2017 ,		1
40	Dynamic Model of Switched-Capacitor DCDC Converters in the Slow-Switching Limit Including Charge Reusing. <i>IEEE Transactions on Power Electronics</i> , 2017 , 32, 5293-5311	7.2	11
39	A Review of CMOS Photodiode Modeling and the Role of the Lateral Photoresponse. <i>IEEE Transactions on Electron Devices</i> , 2016 , 63, 16-25	2.9	8
38	Dynamic joint model of capacitive charge pumps and on-chip photovoltaic cells for CMOS micro-energy harvesting. <i>International Journal of Circuit Theory and Applications</i> , 2016 , 44, 1874-1894	2	5
37	Study of the thermoelectric properties of non-typical semiconductor materials with conventional CAD tools 2016 ,		1
36	Design for maximum power transfer efficiency of thermoelectric generators using mixed mode simulations 2016 ,		1

35	Live demonstration: Wireless sensor network for snail pest detection 2016 ,		1
34	Four-transistor pinned photodiodes in standard CMOS technologies for time-of-flight sensors. <i>Semiconductor Science and Technology</i> , 2015 , 30, 045002	1.8	2
33	Distance measurement error in time-of-flight sensors due to shot noise. <i>Sensors</i> , 2015 , 15, 4624-42	3.8	16
32	Capacitance-based wireless sensor mote for snail pest detection 2015 ,		2
31	Analytical Model for Crosstalk in p-nwell Photodiodes. <i>IEEE Transactions on Electron Devices</i> , 2015 , 62, 580-586	2.9	4
30	The dickson charge pump as voltage booster for light energy harvesting on CMOS vision chips 2014 ,		2
29	Simplification and hardware implementation of the feature descriptor vector calculation in the SIFT algorithm 2014 ,		2
28	Dark current in standard CMOS pinned photodiodes for Time-of-Flight sensors 2014 ,		2
27	Wireless sensor mote for snail pest detection 2014 ,		6
26	Closed-Form and Explicit Analytical Model for Crosstalk in CMOS Photodiodes. <i>IEEE Transactions on Electron Devices</i> , 2013 , 60, 3459-3464	2.9	7
25	Experimental characterization of peripheral photocurrent in CMOS photodiodes down to 65 nm technology. <i>Semiconductor Science and Technology</i> , 2013 , 28, 045011	1.8	3
24	Analytical modelling of size effects on the lateral photoresponse of CMOS photodiodes. <i>Solid-State Electronics</i> , 2012 , 73, 15-20	1.7	8
23	A Verilog-AMS photodiode model including lateral effects. <i>Microelectronics Journal</i> , 2012 , 43, 980-984	1.8	10
22	2011 ,		1
21	FPGA computation of the 3D heat equation. <i>Computational Geosciences</i> , 2010 , 14, 649-664	2.7	
20	Non-destructive soil inspection using an efficient 3D softwareHardware heat equation solver. <i>Inverse Problems in Science and Engineering</i> , 2009 , 17, 755-775	1.3	
19	A study of CMOS radiation tolerant transistors using green functions 2009 ,		1
18	Efficient softwareHardware 3D heat equation solver with applications on the non-destructive evaluation of minefields. <i>Computers and Geosciences</i> , 2009 , 35, 2239-2249	4.5	1

17	A dc I _V model for short-channel polygonal enclosed-layout transistors. <i>International Journal of Circuit Theory and Applications</i> , 2009 , 37, 163-177	2	2
16	Analytical model of short-channel gate enclosed transistors using Green functions. <i>Solid-State Electronics</i> , 2009 , 53, 514-519	1.7	1
15	A 2D model for radiation-hard CMOS annular transistors. <i>Semiconductor Science and Technology</i> , 2009 , 24, 125009	1.8	3
14	FPGA-based hardware accelerator of the heat equation with applications on infrared thermography 2008 ,		2
13	DT-CNN emulator: 3D heat equation solver with applications on the non-destructive soil inspection 2008 ,		1
12	Bottom collection of photodiode-based CMOS APS 2008 ,		2
11	Soft-Hard 3D FD-TD Solver for Non Destructive Evaluation 2007 ,		3
10	Improved Analytical I-V model for polygonal-shape enclosed layout transistors 2007 ,		3
9	FPGA Implementation of 3-D Thermal Model Simulator 2006 ,		2
8	Thermal infrared identification of buried landmines 2005 , 5794, 198		5
7	Improved thermal analysis of buried landmines. <i>IEEE Transactions on Geoscience and Remote Sensing</i> , 2004 , 42, 1965-1975	8.1	15
6	Robustness oriented design tool for multilayer DTCNN applications. <i>International Journal of Circuit Theory and Applications</i> , 2002 , 30, 195-210	2	4
5	Genetic algorithm based training for multilayer discrete-time cellular neural networks. <i>Lecture Notes in Computer Science</i> , 1999 , 467-476	0.9	1
4	Performance analysis of high-speed MOS transistors with different layout styles		8
3	CNN-based 3D thermal modeling of the soil for antipersonnel mine detection		4
2	Antipersonnel mine detection on infrared images		1
1	Design and training of multilayer discrete time cellular neural networks for antipersonnel mine detection using genetic algorithms		5