

# Anirban Sengupta

## List of Publications by Year in Descending Order

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

75  
papers

549  
citations

13  
h-index

19  
g-index

94  
ext. papers

699  
ext. citations

2.8  
avg, IF

4.94  
L-index

#	Paper	IF	Citations
75	Hardware (IP) Watermarking During Behavioral Synthesis <b>2022</b> , 119-145		
74	Palmpoint Biometric vs Encrypted Hash based Digital Signature for Securing DSP Cores Used in CE systems. <i>IEEE Consumer Electronics Magazine</i> , <b>2022</b> , 1-1	3.2	
73	Securing IP Cores for DSP applications using Structural Obfuscation and Chromosomal DNA Impression. <i>IEEE Access</i> , <b>2022</b> , 1-1	3.5	
72	Particle Swarm Optimization-Driven DSE-Based Low-Cost Hardware Security for Securing DSP IP Cores. <i>EAI/Springer Innovations in Communication and Computing</i> , <b>2022</b> , 29-54	0.6	
71	An Overview of Hardware Security and Trust: Threats, Countermeasures, and Design Tools. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2021</b> , 40, 1010-1038	2.5	13
70	. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2021</b> , 29, 112-123	2.6	1
69	Contact-Less Palmpoint Biometric for Securing DSP Coprocessors Used in CE Systems. <i>IEEE Transactions on Consumer Electronics</i> , <b>2021</b> , 67, 202-213	4.8	1
68	Securing Hardware Accelerators Using Multi-Key Based Structural Obfuscation. <i>IEEE Letters of the Computer Society</i> , <b>2020</b> , 3, 21-24	0.9	2
67	. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2020</b> , 28, 1979-1992	2.6	5
66	. <i>IEEE Transactions on Consumer Electronics</i> , <b>2020</b> , 66, 251-260	4.8	9
65	Design Flow of Secured N-Point DFT Application Specific Processor Using Obfuscation and Steganography. <i>IEEE Letters of the Computer Society</i> , <b>2020</b> , 3, 13-16	0.9	1
64	Enhanced Security of DSP Circuits Using Multi-Key Based Structural Obfuscation and Physical-Level Watermarking for Consumer Electronics Systems. <i>IEEE Transactions on Consumer Electronics</i> , <b>2020</b> , 66, 163-172	4.8	6
63	Structural Obfuscation and Crypto-Steganography-Based Secured JPEG Compression Hardware for Medical Imaging Systems. <i>IEEE Access</i> , <b>2020</b> , 8, 6543-6565	3.5	8
62	Obfuscated Hardware Accelerators for Image Processing Filters Application Specific and Functionally Reconfigurable Processors. <i>IEEE Transactions on Consumer Electronics</i> , <b>2020</b> , 66, 386-395	4.8	3
61	HLS Based IP Protection of Reusable Cores Using Biometric Fingerprint. <i>IEEE Letters of the Computer Society</i> , <b>2020</b> , 3, 42-45	0.9	
60	Robust Logic locking for Securing Reusable DSP Cores. <i>IEEE Access</i> , <b>2019</b> , 7, 120052-120064	3.5	1
59	Impact of hardware steganography on DSP core datapath. <i>CSI Transactions on ICT</i> , <b>2019</b> , 7, 137-140	0.4	

58	Digital Processing Core Performance Degradation Due to Hardware Stress Attacks. <i>IEEE Potentials</i> , <b>2019</b> , 38, 39-45	1	1
57	Multilevel Watermark for Protecting DSP Kernel in CE Systems [Hardware Matters]. <i>IEEE Consumer Electronics Magazine</i> , <b>2019</b> , 8, 100-102	3.2	1
56	Embedding Digital Signature Using Encrypted-Hashing for Protection of DSP Cores in CE. <i>IEEE Transactions on Consumer Electronics</i> , <b>2019</b> , 65, 398-407	4.8	8
55	Crypto-Based Dual-Phase Hardware Steganography for Securing IP cores. <i>IEEE Letters of the Computer Society</i> , <b>2019</b> , 2, 32-35	0.9	6
54	Low Cost Dual-Phase Watermark for Protecting CE Devices in IoT Framework. <i>Internet of Things</i> , <b>2019</b> , 21-41	1.3	
53	IP Core Steganography for Protecting DSP Kernels Used in CE Systems. <i>IEEE Transactions on Consumer Electronics</i> , <b>2019</b> , 65, 506-515	4.8	10
52	Fault-Tolerant DSP Core Datapath Against Omnidirectional Spatial Impact of SET. <i>Canadian Journal of Electrical and Computer Engineering</i> , <b>2019</b> , 42, 102-107	1.4	1
51	Signature-Free Watermark for Protecting Digital Signal Processing Cores Used in CE Devices [Hardware Matters]. <i>IEEE Consumer Electronics Magazine</i> , <b>2019</b> , 8, 92-94	3.2	12
50	Protecting DSP Kernels Using Robust Hologram-Based Obfuscation. <i>IEEE Transactions on Consumer Electronics</i> , <b>2019</b> , 65, 99-108	4.8	2
49	Security of Functionally Obfuscated DSP Core Against Removal Attack Using SHA-512 Based Key Encryption Hardware. <i>IEEE Access</i> , <b>2019</b> , 7, 4598-4610	3.5	3
48	Low Cost Functional Obfuscation of Reusable IP Cores Used in CE Hardware Through Robust Locking. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2019</b> , 38, 604-616	2.5	8
47	Intellectual Property-Based Lossless Image Compression for Camera Systems [Hardware Matters]. <i>IEEE Consumer Electronics Magazine</i> , <b>2018</b> , 7, 119-124	3.2	4
46	Obfuscated JPEG Image Decompression IP Core for Protecting Against Reverse Engineering [Hardware Matter]. <i>IEEE Consumer Electronics Magazine</i> , <b>2018</b> , 7, 104-109	3.2	
45	Shielding CE Hardware Against Reverse-Engineering Attacks Through Functional Locking [Hardware Matters]. <i>IEEE Consumer Electronics Magazine</i> , <b>2018</b> , 7, 111-114	3.2	4
44	A Framework for Hardware Efficient Reusable IP Core for Grayscale Image CODEC. <i>IEEE Access</i> , <b>2018</b> , 6, 871-882	3.5	2
43	Multi-phase watermark for IP core protection <b>2018</b> ,		1
42	Reusable intellectual property core protection for both buyer and seller <b>2018</b> ,		1
41	. <i>IEEE Transactions on Aerospace and Electronic Systems</i> , <b>2018</b> , 54, 1168-1183	3.7	5

40	Forensic engineering for resolving ownership problem of reusable IP core generated during high level synthesis. <i>Future Generation Computer Systems</i> , <b>2018</b> , 80, 29-46	7.5	1
39	Low-Cost Obfuscated JPEG CODEC IP Core for Secure CE Hardware. <i>IEEE Transactions on Consumer Electronics</i> , <b>2018</b> , 64, 365-374	4.8	12
38	Multi-Phase Obfuscation of Fault Secured DSP Designs With Enhanced Security Feature. <i>IEEE Transactions on Consumer Electronics</i> , <b>2018</b> , 64, 356-364	4.8	5
37	Functional Obfuscation of DSP Cores Using Robust Logic Locking and Encryption <b>2018</b> ,		3
36	Obfuscation of Fault Secured DSP Design Through Hybrid Transformation <b>2018</b> ,		1
35	Audio and Video Technologies: Recent Advances in Consumer Electronics. <i>IEEE Consumer Electronics Magazine</i> , <b>2018</b> , 7, 26-26	3.2	1
34	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2018</b> , 37, 742-755	2.5	16
33	Effect of NBTI stress on DSP cores used in CE devices: threat model and performance estimation. <i>IET Computers and Digital Techniques</i> , <b>2018</b> , 12, 268-278	0.9	2
32	Optimizing DSP Cores Using Design Transformation [Hardware Matters]. <i>IEEE Consumer Electronics Magazine</i> , <b>2018</b> , 7, 91-94	3.2	2
31	Low overhead symmetrical protection of reusable IP core using robust fingerprinting and watermarking during high level synthesis. <i>Future Generation Computer Systems</i> , <b>2017</b> , 71, 89-101	7.5	11
30	Hardware Vulnerabilities and Their Effects on CE Devices: Design for Security Against Trojans [Hardware Matters]. <i>IEEE Consumer Electronics Magazine</i> , <b>2017</b> , 6, 126-133	3.2	10
29	. <i>IEEE Consumer Electronics Magazine</i> , <b>2017</b> , 6, 83-91	3.2	36
28	Antipiracy-Aware IP Chipset Design for CE Devices: A Robust Watermarking Approach [Hardware Matters]. <i>IEEE Consumer Electronics Magazine</i> , <b>2017</b> , 6, 118-124	3.2	16
27	Hardware Security of CE Devices [Hardware Matters]. <i>IEEE Consumer Electronics Magazine</i> , <b>2017</b> , 6, 130-133	3.2	15
26	Low-cost security aware HLS methodology. <i>IET Computers and Digital Techniques</i> , <b>2017</b> , 11, 68-79	0.9	4
25	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , <b>2017</b> , 36, 655-668	2.5	38
24	. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2017</b> , 25, 3265-3267	2.6	13
23	DSP design protection in CE through algorithmic transformation based structural obfuscation. <i>IEEE Transactions on Consumer Electronics</i> , <b>2017</b> , 63, 467-476	4.8	25

22	Mathematical Validation of HWT Based Lossless Image Compression <b>2017</b> ,		1
21	Particle swarm optimisation driven low cost single event transient fault secured design during architectural synthesis. <i>Journal of Engineering</i> , <b>2017</b> , 2017, 184-194	0.7	2
20	Embedding low cost optimal watermark during high level synthesis for reusable IP core protection <b>2016</b> ,		11
19	Exploring Low Cost Optimal Watermark for Reusable IP Cores During High Level Synthesis. <i>IEEE Access</i> , <b>2016</b> , 4, 2198-2215	3.5	37
18	Integrating physical level design and high level synthesis for simultaneous multi-cycle transient and multiple transient fault resiliency of application specific datapath processors. <i>Microelectronics Reliability</i> , <b>2016</b> , 60, 141-152	1.2	8
17	Intellectual Property Cores: Protection designs for CE products. <i>IEEE Consumer Electronics Magazine</i> , <b>2016</b> , 5, 83-88	3.2	12
16	Design Flow of a Digital IC: The role of digital IC/SOC design in CE products. <i>IEEE Consumer Electronics Magazine</i> , <b>2016</b> , 5, 58-62	3.2	7
15	Swarm intelligence driven design space exploration of optimal k-cycle transient fault secured datapath during high level synthesis based on user powerdelay budget. <i>Microelectronics Reliability</i> , <b>2015</b> , 55, 990-1004	1.2	9
14	Adaptive bacterial foraging driven datapath optimization: Exploring power-performance tradeoff in high level synthesis. <i>Applied Mathematics and Computation</i> , <b>2015</b> , 269, 265-278	2.7	8
13	GA driven integrated exploration of loop unrolling factor and datapath for optimal scheduling of CFGs during high level synthesis <b>2015</b> ,		2
12	Exploration of optimal multi-cycle transient fault secured datapath during high level synthesis based on user area-delay budget <b>2015</b> ,		1
11	Swarm Intelligence Driven Simultaneous Adaptive Exploration of Datapath and Loop Unrolling Factor during Area-Performance Tradeoff <b>2014</b> ,		8
10	MO-PSE: Adaptive multi-objective particle swarm optimization based design space exploration in architectural synthesis for application specific processor design. <i>Advances in Engineering Software</i> , <b>2014</b> , 67, 111-124	3.6	35
9	Exploration of Multi-objective Tradeoff during High Level Synthesis Using Bacterial Chemotaxis and Dispersal. <i>Procedia Computer Science</i> , <b>2014</b> , 35, 63-72	1.6	8
8	Time Varying vs. Fixed Acceleration Coefficient PSO Driven Exploration during High Level Synthesis: Performance and Quality Assessment <b>2014</b> ,		2
7	Integrated particle swarm optimization (i-PSO): An adaptive design space exploration framework for power-performance tradeoff in architectural synthesis <b>2014</b> ,		13
6	Automated exploration of datapath and unrolling factor during powerperformance tradeoff in architectural synthesis using multi-dimensional PSO algorithm. <i>Expert Systems With Applications</i> , <b>2014</b> , 41, 4691-4703	7.8	12
5	Execution time - area tradeoff in gausing residual load decoder: Integrated exploration of chaining based schedule and allocation in HLS for hardware accelerators. <i>Facta Universitatis - Series Electronics and Energetics</i> , <b>2014</b> , 27, 235-249	0.4	1

4	Rapid exploration of cost-performance tradeoffs using dominance effect during design of hardware accelerators. <i>Facta Universitatis - Series Electronics and Energetics</i> , <b>2014</b> , 27, 317-328	0.4	1
3	Rapid search of Pareto fronts using D-logic exploration during multi-objective tradeoff of computation intensive applications <b>2013</b> ,		1
2	A multi structure genetic algorithm for integrated design space exploration of scheduling and allocation in high level synthesis for DSP kernels. <i>Swarm and Evolutionary Computation</i> , <b>2012</b> , 7, 35-46	9.8	20
1	A high level synthesis design flow with a novel approach for efficient design space exploration in case of multi-parametric optimization objective. <i>Microelectronics Reliability</i> , <b>2010</b> , 50, 424-437	1.2	17