Anirban Sengupta

List of Publications by Citations

75 papers	549 citations	13 h-index	19 g-index
94 ext. papers	699 ext. citations	2.8 avg, IF	4.94 L-index

#	Paper	IF	Citations
75	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 655-668	2.5	38
74	Exploring Low Cost Optimal Watermark for Reusable IP Cores During High Level Synthesis. *IEEE Access*, **2016**, 4, 2198-2215	3.5	37
73	. *IEEE Consumer Electronics Magazine*, **2017**, 6, 83-91	3.2	36
72	MO-PSE: Adaptive multi-objective particle swarm optimization based design space exploration in architectural synthesis for application specific processor design. *Advances in Engineering Software*, **2014**, 67, 111-124	3.6	35
71	DSP design protection in CE through algorithmic transformation based structural obfuscation. *IEEE Transactions on Consumer Electronics*, **2017**, 63, 467-476	4.8	25
70	A multi structure genetic algorithm for integrated design space exploration of scheduling and allocation in high level synthesis for DSP kernels. *Swarm and Evolutionary Computation*, **2012**, 7, 35-46	9.8	20
69	A high level synthesis design flow with a novel approach for efficient design space exploration in case of multi-parametric optimization objective. *Microelectronics Reliability*, **2010**, 50, 424-437	1.2	17
68	Antipiracy-Aware IP Chipset Design for CE Devices: A Robust Watermarking Approach [Hardware Matters]. *IEEE Consumer Electronics Magazine*, **2017**, 6, 118-124	3.2	16
67	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 742-755	2.5	16
66	Hardware Security of CE Devices [Hardware Matters]. *IEEE Consumer Electronics Magazine*, **2017**, 6, 130-133	3.2	15
65	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 3265-3267	2.6	13
64	Integrated particle swarm optimization (i-PSO): An adaptive design space exploration framework for power-performance tradeoff in architectural synthesis **2014**,		13
63	An Overview of Hardware Security and Trust: Threats, Countermeasures, and Design Tools. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 1010-1038	2.5	13
62	Intellectual Property Cores: Protection designs for CE products. *IEEE Consumer Electronics Magazine*, **2016**, 5, 83-88	3.2	12
61	Low-Cost Obfuscated JPEG CODEC IP Core for Secure CE Hardware. *IEEE Transactions on Consumer Electronics*, **2018**, 64, 365-374	4.8	12
60	Automated exploration of datapath and unrolling factor during power performance tradeoff in architectural synthesis using multi-dimensional PSO algorithm. *Expert Systems With Applications*, **2014**, 41, 4691-4703	7.8	12
59	Signature-Free Watermark for Protecting Digital Signal Processing Cores Used in CE Devices [Hardware Matters]. *IEEE Consumer Electronics Magazine*, **2019**, 8, 92-94	3.2	12

58	Low overhead symmetrical protection of reusable IP core using robust fingerprinting and watermarking during high level synthesis. *Future Generation Computer Systems*, **2017**, 71, 89-101	7.5	11
57	Embedding low cost optimal watermark during high level synthesis for reusable IP core protection **2016**,		11
56	Hardware Vulnerabilities and Their Effects on CE Devices: Design for Security Against Trojans [Hardware Matters]. *IEEE Consumer Electronics Magazine*, **2017**, 6, 126-133	3.2	10
55	IP Core Steganography for Protecting DSP Kernels Used in CE Systems. *IEEE Transactions on Consumer Electronics*, **2019**, 65, 506-515	4.8	10
54	Swarm intelligence driven design space exploration of optimal k-cycle transient fault secured datapath during high level synthesis based on user power□delay budget. *Microelectronics Reliability* , **2015**, 55, 990-1004	1.2	9
53	. *IEEE Transactions on Consumer Electronics*, **2020**, 66, 251-260	4.8	9
52	Adaptive bacterial foraging driven datapath optimization: Exploring power-performance tradeoff in high level synthesis. *Applied Mathematics and Computation*, **2015**, 269, 265-278	2.7	8
51	Integrating physical level design and high level synthesis for simultaneous multi-cycle transient and multiple transient fault resiliency of application specific datapath processors. *Microelectronics Reliability*, **2016**, 60, 141-152	1.2	8
50	Embedding Digital Signature Using Encrypted-Hashing for Protection of DSP Cores in CE. *IEEE Transactions on Consumer Electronics*, **2019**, 65, 398-407	4.8	8
49	Swarm Intelligence Driven Simultaneous Adaptive Exploration of Datapath and Loop Unrolling Factor during Area-Performance Tradeoff **2014**,		8
48	Exploration of Multi-objective Tradeoff during High Level Synthesis Using Bacterial Chemotaxis and Dispersal. *Procedia Computer Science*, **2014**, 35, 63-72	1.6	8
47	Structural Obfuscation and Crypto-Steganography-Based Secured JPEG Compression Hardware for Medical Imaging Systems. *IEEE Access*, **2020**, 8, 6543-6565	3.5	8
46	Low Cost Functional Obfuscation of Reusable IP Cores Used in CE Hardware Through Robust Locking. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 604-616	2.5	8
45	Design Flow of a Digital IC: The role of digital IC/SOC design in CE products. *IEEE Consumer Electronics Magazine*, **2016**, 5, 58-62	3.2	7
44	Enhanced Security of DSP Circuits Using Multi-Key Based Structural Obfuscation and Physical-Level Watermarking for Consumer Electronics Systems. *IEEE Transactions on Consumer Electronics*, **2020**, 66, 163-172	4.8	6
43	Crypto-Based Dual-Phase Hardware Steganography for Securing IP cores. *IEEE Letters of the Computer Society*, **2019**, 2, 32-35	0.9	6
42	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 1979-1992	2.6	5
41	. *IEEE Transactions on Aerospace and Electronic Systems*, **2018**, 54, 1168-1183	3.7	5

40	Multi-Phase Obfuscation of Fault Secured DSP Designs With Enhanced Security Feature. *IEEE Transactions on Consumer Electronics*, **2018**, 64, 356-364	4.8	5
39	Intellectual Property-Based Lossless Image Compression for Camera Systems [Hardware Matters]. *IEEE Consumer Electronics Magazine*, **2018**, 7, 119-124	3.2	4
38	Shielding CE Hardware Against Reverse-Engineering Attacks Through Functional Locking [Hardware Matters]. *IEEE Consumer Electronics Magazine*, **2018**, 7, 111-114	3.2	4
37	Low-cost security aware HLS methodology. *IET Computers and Digital Techniques*, **2017**, 11, 68-79	0.9	4
36	Functional Obfuscation of DSP Cores Using Robust Logic Locking and Encryption **2018**,		3
35	Obfuscated Hardware Accelerators for Image Processing Filters[A]pplication Specific and Functionally Reconfigurable Processors. *IEEE Transactions on Consumer Electronics*, **2020**, 66, 386-395	4.8	3
34	Security of Functionally Obfuscated DSP Core Against Removal Attack Using SHA-512 Based Key Encryption Hardware. *IEEE Access*, **2019**, 7, 4598-4610	3.5	3
33	Securing Hardware Accelerators Using Multi-Key Based Structural Obfuscation. *IEEE Letters of the Computer Society*, **2020**, 3, 21-24	0.9	2
32	A Framework for Hardware Efficient Reusable IP Core for Grayscale Image CODEC. *IEEE Access*, **2018**, 6, 871-882	3.5	2
31	Particle swarm optimisation driven low cost single event transient fault secured design during architectural synthesis. *Journal of Engineering*, **2017**, 2017, 184-194	0.7	2
30	GA driven integrated exploration of loop unrolling factor and datapath for optimal scheduling of CDFGs during high level synthesis **2015**,		2
29	Time Varying vs. Fixed Acceleration Coefficient PSO Driven Exploration during High Level Synthesis: Performance and Quality Assessment **2014**,		2
28	Protecting DSP Kernels Using Robust Hologram-Based Obfuscation. *IEEE Transactions on Consumer Electronics*, **2019**, 65, 99-108	4.8	2
27	Effect of NBTI stress on DSP cores used in CE devices: threat model and performance estimation. *IET Computers and Digital Techniques*, **2018**, 12, 268-278	0.9	2
26	Optimizing DSP Cores Using Design Transformation [Hardware Matters]. *IEEE Consumer Electronics Magazine*, **2018**, 7, 91-94	3.2	2
25	Robust Logic locking for Securing Reusable DSP Cores. *IEEE Access*, **2019**, 7, 120052-120064	3.5	1
24	Digital Processing Core Performance Degradation Due to Hardware Stress Attacks. *IEEE Potentials*, **2019**, 38, 39-45	1	1
23	Multilevel Watermark for Protecting DSP Kernel in CE Systems [Hardware Matters]. *IEEE Consumer Electronics Magazine*, **2019**, 8, 100-102	3.2	1

22	Design Flow of Secured N-Point DFT Application Specific Processor Using Obfuscation and Steganography. *IEEE Letters of the Computer Society*, **2020**, 3, 13-16	0.9	1
21	Multi-phase watermark for IP core protection **2018**,		1
20	Reusable intellectual property core protection for both buyer and seller **2018**,		1
19	Forensic engineering for resolving ownership problem of reusable IP core generated during high level synthesis. *Future Generation Computer Systems*, **2018**, 80, 29-46	7.5	1
18	Obfuscation of Fault Secured DSP Design Through Hybrid Transformation **2018**,		1
17	Audio and Video Technologies: Recent Advances in Consumer Electronics. *IEEE Consumer Electronics Magazine*, **2018**, 7, 26-26	3.2	1
16	Rapid search of Pareto fronts using D-logic exploration during multi-objective tradeoff of computation intensive applications **2013**,		1
15	Mathematical Validation of HWT Based Lossless Image Compression **2017**,		1
14	Exploration of optimal multi-cycle transient fault secured datapath during high level synthesis based on user area-delay budget **2015**,		1
13	Execution time - area tradeoff in gausing residual load decoder: Integrated exploration of chaining based schedule and allocation in HLS for hardware accelerators. *Facta Universitatis - Series Electronics and Energetics*, **2014**, 27, 235-249	0.4	1
12	Rapid exploration of cost-performance tradeoffs using dominance effect during design of hardware accelerators. *Facta Universitatis - Series Electronics and Energetics*, **2014**, 27, 317-328	0.4	1
11	Fault-Tolerant DSP Core Datapath Against Omnidirectional Spatial Impact of SET. *Canadian Journal of Electrical and Computer Engineering*, **2019**, 42, 102-107	1.4	1
10	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 112-123	2.6	1
9	Contact-Less Palmprint Biometric for Securing DSP Coprocessors Used in CE Systems. *IEEE Transactions on Consumer Electronics*, **2021**, 67, 202-213	4.8	1
8	Impact of hardware steganography on DSP core datapath. *CSI Transactions on ICT*, **2019**, 7, 137-140	0.4	
7	Obfuscated JPEG Image Decompression IP Core for Protecting Against Reverse Engineering [Hardware Matter]. *IEEE Consumer Electronics Magazine*, **2018**, 7, 104-109	3.2	
6	Hardware (IP) Watermarking During Behavioral Synthesis **2022**, 119-145		
5	Low Cost Dual-Phase Watermark for Protecting CE Devices in IoT Framework. *Internet of Things*, **2019**, 21-41	1.3	

4	HLS Based IP Protection of Reusable Cores Using Biometric Fingerprint. *IEEE Letters of the Computer Society*, **2020**, 3, 42-45	0.9
3	Palmprint Biometric vs Encrypted Hash based Digital Signature for Securing DSP Cores Used in CE systems. *IEEE Consumer Electronics Magazine*, **2022**, 1-1	3.2
2	Securing IP Cores for DSP applications using Structural Obfuscation and Chromosomal DNA Impression. *IEEE Access*, **2022**, 1-1	3.5
1	Particle Swarm Optimization-Driven DSE-Based Low-Cost Hardware Security for Securing DSP IP Cores. *EAI/Springer Innovations in Communication and Computing*, **2022**, 29-54	0.6