Anirban Sengupta

List of Publications by Year
in descending order

93	875	471061 17	552369 26
papers	citations	h-index	g-index

94	94	94	397
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	An Overview of Hardware Security and Trust: Threats, Countermeasures, and Design Tools. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1010-1038.	1.9	56
2	TL-HLS: Methodology for Low Cost Hardware Trojan Security Aware Scheduling With Optimal Loop Unrolling Factor During High Level Synthesis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 655-668.	1.9	54
3	Exploring Low Cost Optimal Watermark for Reusable IP Cores During High Level Synthesis. IEEE Access, 2016, 4, 2198-2215.	2.6	50
4	MO-PSE: Adaptive multi-objective particle swarm optimization based design space exploration in architectural synthesis for application specific processor design. Advances in Engineering Software, 2014, 67, 111-124.	1.8	49
5	Everything You Want to Know About Watermarking: From Paper Marks to Hardware Protection. IEEE Consumer Electronics Magazine, 2017, 6, 83-91.	2.3	44
6	DSP design protection in CE through algorithmic transformation based structural obfuscation. IEEE Transactions on Consumer Electronics, 2017, 63, 467-476.	3.0	37
7	A multi structure genetic algorithm for integrated design space exploration of scheduling and allocation in high level synthesis for DSP kernels. Swarm and Evolutionary Computation, 2012, 7, 35-46.	4.5	30
8	Triple-Phase Watermarking for Reusable IP Core Protection During Architecture Synthesis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 742-755.	1.9	28
9	A high level synthesis design flow with a novel approach for efficient design space exploration in case of multi-parametric optimization objective. Microelectronics Reliability, 2010, 50, 424-437.	0.9	24
10	IP Core Steganography for Protecting DSP Kernels Used in CE Systems. IEEE Transactions on Consumer Electronics, 2019, 65, 506-515.	3.0	23
11	Embedding Digital Signature Using Encrypted-Hashing for Protection of DSP Cores in CE. IEEE Transactions on Consumer Electronics, 2019, 65, 398-407.	3.0	21
12	IP Core Steganography Using Switch Based Key-Driven Hash-Chaining and Encoding for Securing DSP Kernels Used in CE Systems. IEEE Transactions on Consumer Electronics, 2020, 66, 251-260.	3.0	21
13	Antipiracy-Aware IP Chipset Design for CE Devices: A Robust Watermarking Approach [Hardware Matters]. IEEE Consumer Electronics Magazine, 2017, 6, 118-124.	2.3	19
14	Embedding low cost optimal watermark during high level synthesis for reusable IP core protection. , 2016, , .		18
15	Guest Editorial Securing IoT Hardware: Threat Models and Reliable, Low-Power Design Solutions. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3265-3267.	2.1	18
16	Low-Cost Obfuscated JPEG CODEC IP Core for Secure CE Hardware. IEEE Transactions on Consumer Electronics, 2018, 64, 365-374.	3.0	18
17	Signature-Free Watermark for Protecting Digital Signal Processing Cores Used in CE Devices [Hardware Matters]. IEEE Consumer Electronics Magazine, 2019, 8, 92-94.	2.3	18
18	Hardware Security of CE Devices [Hardware Matters]. IEEE Consumer Electronics Magazine, 2017, 6, 130-133.	2.3	17

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19	Intellectual Property Cores: Protection designs for CE products. IEEE Consumer Electronics Magazine, 2016, 5, 83-88.	2.3	16
20	Low overhead symmetrical protection of reusable IP core using robust fingerprinting and watermarking during high level synthesis. Future Generation Computer Systems, 2017, 71, 89-101.	4.9	16
21	Structural Obfuscation and Crypto-Steganography-Based Secured JPEG Compression Hardware for Medical Imaging Systems. IEEE Access, 2020, 8, 6543-6565.	2.6	16
22	Integrated particle swarm optimization (i-PSO): An adaptive design space exploration framework for power-performance tradeoff in architectural synthesis. , 2014, , .		15
23	Automated exploration of datapath and unrolling factor during powerâ€“performance tradeoff in architectural synthesis using multi-dimensional PSO algorithm. Expert Systems With Applications, 2014, 41, 4691-4703.	4.4	15
24	Securing Hardware Accelerators for CE Systems Using Biometric Fingerprinting. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1979-1992.	2.1	14
25	Integrating physical level design and high level synthesis for simultaneous multi-cycle transient and multiple transient fault resiliency of application specific datapath processors. Microelectronics Reliability, 2016, 60, 141-152.	0.9	13
26	Enhanced Security of DSP Circuits Using Multi-Key Based Structural Obfuscation and Physical-Level Watermarking for Consumer Electronics Systems. IEEE Transactions on Consumer Electronics, 2020, 66, 163-172.	3.0	13
27	Swarm intelligence driven design space exploration of optimal k-cycle transient fault secured datapath during high level synthesis based on user powerâ€“delay budget. Microelectronics Reliability, 2015, 55, 990-1004.	0.9	12
28	Hardware Vulnerabilities and Their Effects on CE Devices: Design for Security Against Trojans [Hardware Matters]. IEEE Consumer Electronics Magazine, 2017, 6, 126-133.	2.3	12
29	Low Cost Functional Obfuscation of Reusable IP Cores Used in CE Hardware Through Robust Locking. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 604-616.	1.9	12
30	Exploration of Multi-objective Tradeoff during High Level Synthesis Using Bacterial Chemotaxis and Dispersal. Procedia Computer Science, 2014, 35, 63-72.	1.2	11
31	Swarm Intelligence Driven Simultaneous Adaptive Exploration of Datapath and Loop Unrolling Factor during Area-Performance Tradeoff. , 2014, , .		10
32	Adaptive bacterial foraging driven datapath optimization: Exploring power-performance tradeoff in high level synthesis. Applied Mathematics and Computation, 2015, 269, 265-278.	1.4	10
33	Facial Biometric for Securing Hardware Accelerators. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 112-123.	2.1	10
34	Design Flow of a Digital IC: The role of digital IC/SOC design in CE products. IEEE Consumer Electronics Magazine, 2016, 5, 58-62.	2.3	9
35	Multi-Phase Obfuscation of Fault Secured DSP Designs With Enhanced Security Feature. IEEE Transactions on Consumer Electronics, 2018, 64, 356-364.	3.0	9
36	Crypto-Based Dual-Phase Hardware Steganography for Securing IP cores. IEEE Letters of the Computer Society, 2019, 2, 32-35.	1.1	9

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37	Intellectual Property-Based Lossless Image Compression for Camera Systems [Hardware Matters]. IEEE Consumer Electronics Magazine, 2018, 7, 119-124.	2.3	7
38	Contact-Less Palmprint Biometric for Securing DSP Coprocessors Used in CE Systems. IEEE Transactions on Consumer Electronics, 2021, 67, 202-213.	3.0	7
39	Spatial and Temporal Redundancy for Transient Fault-Tolerant Datapath. IEEE Transactions on Aerospace and Electronic Systems, 2018, 54, 1168-1183.	2.6	6
40	Securing IP Cores for DSP Applications Using Structural Obfuscation and Chromosomal DNA Impression. IEEE Access, 2022, 10, 50903-50913.	2.6	6
41	Protecting DSP Kernels Using Robust Hologram-Based Obfuscation. IEEE Transactions on Consumer Electronics, 2019, 65, 99-108.	3.0	5
42	Security of Functionally Obfuscated DSP Core Against Removal Attack Using SHA-512 Based Key Encryption Hardware. IEEE Access, 2019, 7, 4598-4610.	2.6	5
43	GA driven integrated exploration of loop unrolling factor and datapath for optimal scheduling of CDFGs during high level synthesis. , 2015, , .		4
44	Generating Multi-cycle and Multiple Transient Fault Resilient Design During Physically Aware High Level Synthesis. , 2016, , .		4
45	Lowâ€cost security aware HLS methodology. IET Computers and Digital Techniques, 2017, 11, 68-79.	0.9	4
46	Shielding CE Hardware Against Reverse-Engineering Attacks Through Functional Locking [Hardware Matters]. IEEE Consumer Electronics Magazine, 2018, 7, 111-114.	2.3	4
47	Functional Obfuscation of DSP Cores Using Robust Logic Locking and Encryption. , 2018, , .		4
48	Obfuscated Hardware Accelerators for Image Processing Filtersâ€"Application Specific and Functionally Reconfigurable Processors. IEEE Transactions on Consumer Electronics, 2020, 66, 386-395.	3.0	4
49	Secured Convolutional Layer IP Core in Convolutional Neural Network Using Facial Biometric. IEEE Transactions on Consumer Electronics, 2022, 68, 291-306.	3.0	4
50	Time Varying vs. Fixed Acceleration Coefficient PSO Driven Exploration during High Level Synthesis: Performance and Quality Assessment. , 2014, , .		3
51	A Framework for Hardware Efficient Reusable IP Core for Grayscale Image CODEC. IEEE Access, 2018, 6, 871-882.	2.6	3
52	Particle swarm optimisation driven low cost single event transient fault secured design during architectural synthesis. Journal of Engineering, 2017, 2017, 184-194.	0.6	2
53	Reusable intellectual property core protection for both buyer and seller. , 2018, , .		2
54	Forensic engineering for resolving ownership problem of reusable IP core generated during high level synthesis. Future Generation Computer Systems, 2018, 80, 29-46.	4.9	2

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55	Effect of NBTI stress on DSP cores used in CE devices: threat model and performance estimation. IET Computers and Digital Techniques, 2018, 12, 268-278.	0.9	2
56	Optimizing DSP Cores Using Design Transformation [Hardware Matters]. IEEE Consumer Electronics Magazine, 2018, 7, 91-94.	2.3	2
57	Audio and Video Technologies: Recent Advances in Consumer Electronics. IEEE Consumer Electronics Magazine, 2018, 7, 26-26.	2.3	2
58	Fault-Tolerant DSP Core Datapath Against Omnidirectional Spatial Impact of SET. Canadian Journal of Electrical and Computer Engineering, 2019, 42, 102-107.	1.5	2
59	HLS Based IP Protection of Reusable Cores Using Biometric Fingerprint. IEEE Letters of the Computer Society, 2020, 3, 42-45.	1.1	2
60	Securing Hardware Accelerators Using Multi-Key Based Structural Obfuscation. IEEE Letters of the Computer Society, 2020, 3, 21-24.	1.1	2
61	Securing IP Cores in CE Systems using Key-driven Hash-chaining based Steganography. , 2020, , .		2
62	Rapid search of Pareto fronts using D-logic exploration during multi-objective tradeoff of computation intensive applications. , 2013, , .		1
63	A methodology for self correction scheme based fast multi criterion exploration and architectual synthesis of data dominated applications. , 2013, , .		1
64	Error Masking of Transient Faults: Exploration of a Fault Tolerant Datapath Based on User Specified Power and Delay Budget. , 2014, , .		1
65	Exploration of optimal multi-cycle transient fault secured datapath during high level synthesis based on user area-delay budget. , 2015, , .		1
66	Reliability and Threat Analysis of NBTI Stress on DSP Cores. , 2017, , .		1
67	Comprehensive Operation Chaining Based Schedule Delay Estimation During High Level Synthesis. , 2017, , .		1
68	Mathematical Validation of HWT Based Lossless Image Compression. , 2017, , .		1
69	Multi-phase watermark for IP core protection. , 2018, , .		1
70	Obfuscation of Fault Secured DSP Design Through Hybrid Transformation. , 2018, , .		1
71	Robust Logic locking for Securing Reusable DSP Cores. IEEE Access, 2019, 7, 120052-120064.	2.6	1
72	Digital Processing Core Performance Degradation Due to Hardware Stress Attacks. IEEE Potentials, 2019, 38, 39-45.	0.2	1

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73	Multilevel Watermark for Protecting DSP Kernel in CE Systems [Hardware Matters]. IEEE Consumer Electronics Magazine, 2019, 8, 100-102.	2.3	1
74	Design Flow of Secured N-Point DFT Application Specific Processor Using Obfuscation and Steganography. IEEE Letters of the Computer Society, 2020, 3, 13-16.	1.1	1
75	Execution time - area tradeoff in gausing residual load decoder: Integrated exploration of chaining based schedule and allocation in HLS for hardware accelerators. Facta Universitatis - Series Electronics and Energetics, 2014, 27, 235-249.	0.6	1
76	Rapid exploration of cost-performance tradeoffs using dominance effect during design of hardware accelerators. Facta Universitatis - Series Electronics and Energetics, 2014, 27, 317-328.	0.6	1
77	Hardware (IP) Watermarking During Behavioral Synthesis. , 2022, , 119-145.		1
78	Palmprint Biometric Versus Encrypted Hash Based Digital Signature for Securing DSP Cores Used in CE Systems. IEEE Consumer Electronics Magazine, 2022, 11, 73-80.	2.3	1
79	Signature Biometric based Authentication of IP Cores for Secure Electronic Systems. , 2021, , .		1
80	Swarm intelligence driven Design Space Exploration: An integrated framework for power-performance trade-off in architectural synthesis. , 2013, , .		0
81	D-logic exploration: Rapid search of Pareto fronts during architectural synthesis of custom processors. , 2013, , .		0
82	A Firefly Algorithm Driven Approach for High Level Synthesis. , 2017, , .		0
83	Obfuscated JPEG Image Decompression IP Core for Protecting Against Reverse Engineering [Hardware Matter]. IEEE Consumer Electronics Magazine, 2018, 7, 104-109.	2.3	0
84	Integrating Compiler Driven Transformation and Simulated Annealing Based Floorplan for Optimized Transient Fault Tolerant DSP Cores. , 2018, , .		0
85	High Level Synthesis Methodology for Exploring Loop Unrolling Factor and Functional Datapath. , 2018, , .		0
86	Impact of hardware steganography on DSP core datapath. CSI Transactions on ICT, 2019, 7, 137-140.	0.7	0
87	Design Pruning of DSP Kernel for Multi Objective IP Core Architecture. , 2019, , .		0
88	Low-Overhead Robust RTL Signature for DSP Core Protection: New Paradigm for Smart CE Design. , 2019, , .		0
89	Robust Digital Signature to Protect IP Core against Fraudulent Ownership and Cloning. , 2019, , .		0
90	Hardware Steganography for IP Core Protection of Fault Secured DSP Cores. , 2019, , .		0

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91	Obfuscating DSP Hardware Accelerators in CE Systems Using Pseudo Operations Mixing. , 2020, , .		0
92	Low Cost Dual-Phase Watermark for Protecting CE Devices in IoT Framework. Internet of Things, 2019, , 21-41.	1.3	0
93	Securing Reusable Hardware IP cores using Palmprint Biometric. , 2021, , .		0