# Jafar Sobhi

List of Publications by Year
in descending order



| 44 | 240 | 1040056 9 | 1058476 14 |
|---|---|---|---|
| papers | citations | h-index | g-index |

| 44 | 44 | 44 | 189 |
|---|---|---|---|
| all docs | docs citations | times ranked | citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | Cost-effective fabrication approaches for improving output performance of triboelectric energy harvesters. Journal of Electrostatics, 2022, 115, 103640. | 1.9 | 6 |
| 2 | Effect of the inherent capacitance optimization on the output performance of triboelectric nanogenerators. Nano Energy, 2022, 92, 106740. | 16.0 | 10 |
| 3 | A low power MASH digital delta-sigma modulator with accurate output average value. Microelectronics Journal, 2022, 121, 105381. | 2.0 | 0 |
| 4 | A new Mylar-based triboelectric energy harvester with an innovative design for mechanical energy harvesting applications. Energy Conversion and Management, 2021, 244, 114489. | 9.2 | 29 |
| 5 | An Open-Loop Time Amplifier With Zero-Gain Delay in Output for Coarse-Fine Time to Digital Converters. , 2021, , . | | 1 |
| 6 | A low power wideband RGC-based modified-MIC trans-impedance amplifier in 0.18Ââ€‹Î¼m CMOS process. Microelectronics Journal, 2020, 96, 104682. | 2.0 | 6 |
| 7 | An 87-dB-SNDR 1MS/s Bilateral Bootstrapped CMOS Switch for Sample-and-Hold Circuit. , 2020, , . | | 4 |
| 8 | Recovery of Oversaturated Pixels in a Low-Cost Solder Paste Inspection Setup. , 2020, , . | | 1 |
| 9 | Application of Folded Cascode-Based Gain-Boosting Circuit in Declining the Current Mismatch Characteristics. , 2020, , . | | 1 |
| 10 | A new direct multiplexing based pulse shaping idea for bandwidth efficient OQPSK transmitters in biomedical applications. Analog Integrated Circuits and Signal Processing, 2020, 102, 523-540. | 1.4 | 0 |
| 11 | A 2.4ÂGHz integer-N frequency synthesizer for ZigBee applications. Analog Integrated Circuits and Signal Processing, 2019, 99, 167-175. | 1.4 | 1 |
| 12 | A FHD 1080, 120 fps CMOS image sensor with two step SS-ADC. Analog Integrated Circuits and Signal Processing, 2019, 99, 339-347. | 1.4 | 1 |
| 13 | Design of Analog Baseband Chain Circuits for IEEE 802.11a/b/g WLAN Receivers. , 2018, , . | | 0 |
| 14 | Design of a reconfigurable frontâ€end for a multistandard receiver for the frequency range of 800ÂMHz to 2.5ÂGHz. International Journal of Circuit Theory and Applications, 2018, 46, 1144-1165. | 2.0 | 3 |
| 15 | An ultraâ€linear CMOS image sensor for a highâ€accuracy imaging system. International Journal of Circuit Theory and Applications, 2018, 46, 1593-1605. | 2.0 | 7 |
| 16 | A sub-mW 2.9-dB noise figure Inductor-less low noise amplifier for wireless sensor network applications. AEU - International Journal of Electronics and Communications, 2018, 93, 132-139. | 2.9 | 10 |
| 17 | A Simple and Efficient Charge Injection Error Compensation Structure for MOS Sampling Switches. Journal of Circuits, Systems and Computers, 2018, 27, 1850130. | 1.5 | 5 |
| 18 | Pre-distortion technique to improve linearity of low noise amplifier. Microelectronics Journal, 2017, 61, 95-105. | 2.0 | 26 |

| # | Article | IF | Citations |
|---|---|---|---|
| 19 | A 500ÂMHz low offset fully differential latched comparator. Analog Integrated Circuits and Signal Processing, 2017, 92, 233-245. | 1.4 | 2 |
| 20 | A linear ultra wide band low noise amplifier using pre-distortion technique. AEU - International Journal of Electronics and Communications, 2017, 79, 172-183. | 2.9 | 22 |
| 21 | Design of efficient power amplifier for low power transmitters. Analog Integrated Circuits and Signal Processing, 2017, 90, 563-571. | 1.4 | 3 |
| 22 | A new high-speed low-power and low-offset dynamic comparator with a current-mode offset compensation technique. AEU - International Journal of Electronics and Communications, 2017, 81, 163-170. | 2.9 | 10 |
| 23 | A sub-2-dB noise figure linear wideband low noise amplifier in 0.18 Âµm CMOS. Microelectronics Journal, 2017, 67, 135-142. | 2.0 | 11 |
| 24 | Very linear open-loop CMOS sample-and-hold structure for high precision and high speed ADCs. Analog Integrated Circuits and Signal Processing, 2016, 88, 23-30. | 1.4 | 3 |
| 25 | Linearity improvement of gm-boosted common gate LNA: Analysis to design. Microelectronics Journal, 2016, 56, 156-162. | 2.0 | 22 |
| 26 | A 670Î¼W inductorless low noise amplifier employing dual capacitive cross coupling and dual negative feedback. , 2016, , . | | 3 |
| 27 | A â^' 10ÂdBm 5ÂMbps Energy-Efficient Injection-Locked FSK Transceiver for Wireless Body Sensor Networks. IETE Journal of Research, 2016, 62, 257-264. | 2.6 | 1 |
| 28 | An Inductor-less Sub-mW Low Noise Amplifier for Wireless Sensor Network Applications. The Integration VLSI Journal, 2016, 52, 316-322. | 2.1 | 13 |
| 29 | A novel topology for modular frequency dividers with enhanced speed and power efficiency. Analog Integrated Circuits and Signal Processing, 2015, 84, 161-171. | 1.4 | 0 |
| 30 | A novel low power high CMRR pseudo-differential CMOS OTA with common-mode feedforward technique. , 2015, , . | | 3 |
| 31 | A linear, low power, 2.5-dB NF LNA for UWB application in a 0.18Î¼m CMOS. Microelectronics Journal, 2015, 46, 1398-1408. | 2.0 | 8 |
| 32 | Efficiency Analysis of Low Power Class-E Power Amplifier. Modern Applied Science, 2014, 8, 19. | 0.6 | 2 |
| 33 | A high speed power efficient pipeline ADC in 0.18μm CMOS. , 2013, , . | | 1 |
| 34 | Ultra low power frequency divider for 2.45ÂGHz ZigBee frequency synthesizer. Analog Integrated Circuits and Signal Processing, 2013, 74, 97-103. | 1.4 | 5 |
| 35 | Nano Watt CMOS temperature sensor. Analog Integrated Circuits and Signal Processing, 2013, 75, 343-348. | 1.4 | 12 |
| 36 | A high efficiency DC-DC Converter using a new in-package structure of Bonding-Wire inductor. IEICE Electronics Express, 2012, 9, 1005-1011. | 0.8 | 2 |

| # | Article | IF | Citations |
|---|---|---|---|
| 37 | A wide-band multipath CMOS OTA for high speed applications. IEICE Electronics Express, 2011, 8, 449-453. | 0.8 | 0 |
| 38 | Design of a 12-bit high-speed CMOS D/A converter using a new 3D digital decoder structure useful for wireless transmitter applications. Analog Integrated Circuits and Signal Processing, 2011, 68, 315-328. | 1.4 | 4 |
| 39 | A Simple Background Interstage Gain Calibration Technique for Pipeline ADCs. , 2009, , . | | 0 |
| 40 | A mixed mode background calibration technique for pipeline ADCs. , 2009, , . | | 0 |
| 41 | Design of a programmable bandgap reference circuit. , 2009, , . | | 1 |
| 42 | A fully digital Background calibration technique for pipeline analog-to-digital converters. , 2009, , . | | 1 |
| 43 | A simple background interstage gain calibration technique for pipeline ADCs. , 2009, , . | | 0 |
| 44 | A lowâ€power wideband LNA exploiting currentâ€reuse and noise cancelation techniques. International Journal of Circuit Theory and Applications, 0, , . | 2.0 | 0 |