Paolo Meloni

List of Publications by Year
in descending order

57	652	623734	677142
papers	citations	14 h-index	22 g-index

58	58	58	510
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	An FPGA Platform for Real-Time Simulation of Spiking Neuronal Networks. Frontiers in Neuroscience, 2017, 11, 90.	2.8	69
2	NoC Design and Implementation in 65nm Technology. , 2007, , .		51
3	NEURA <scp>ghe</scp>. ACM Transactions on Reconfigurable Technology and Systems, 2018, 11, 1-24.	2.5	50
4	A Layout-Aware Analysis of Networks-on-Chip and Traditional Interconnects for MPSoCs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 421-434.	2.7	47
5	Synthesis of Predictable Networks-on-Chip-Based Interconnect Architectures for Chip Multiprocessors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 869-880.	3.1	35
6	Designing Application-Specific Networks on Chips with Floorplan Information. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	26
7	ASAM: Automatic architecture synthesis and application mapping. Microprocessors and Microsystems, 2013, 37, 1002-1019.	2.8	23
8	System Adaptivity and Fault-Tolerance in NoC-based MPSoCs: The MADNESS Project Approach. , 2012, , .		22
9	Area and Power Modeling for Networks-on-Chip with Layout Awareness. VLSI Design, 2007, 2007, 1-12.	0.5	22
10	The multi-dataflow composer tool: generation of on-the-fly reconfigurable platforms. Journal of Real-Time Image Processing, 2014, 9, 233-249.	3.5	21
11	Optimizing Temporal Convolutional Network Inference on FPGA-Based Accelerators. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 348-361.	3.6	21
12	Exploiting All Programmable SoCs in Neural Signal Analysis: A Closed-Loop Control for Large-Scale CMOS Multielectrode Arrays. IEEE Transactions on Biomedical Circuits and Systems, 2018, 12, 839-850.	4.0	17
13	An FPGA-Based Framework for Technology-Aware Prototyping of Multicore Embedded Architectures. IEEE Embedded Systems Letters, 2010, 2, 5-9.	1.9	16
14	Adaptivity Support for MPSoCs Based on Process Migration in Polyhedral Process Networks. VLSI Design, 2012, 2012, 1-17.	0.5	15
15	Challenging the Best HEVC Fractional Pixel FPGA Interpolators With Reconfigurable and Multifrequency Approximate Computing. IEEE Embedded Systems Letters, 2017, 9, 65-68.	1.9	15
16	Automated Design Flow for Multi-Functional Dataflow-Based Platforms. Journal of Signal Processing Systems, 2016, 85, 143-165.	2.1	14
17	Power-Awarness in Coarse-Grained Reconfigurable Multi-Functional Architectures: a Dataflow Based Strategy. Journal of Signal Processing Systems, 2017, 87, 81-106.	2.1	14
18	An Adaptive Cognitive Sensor Node for ECG Monitoring in the Internet of Medical Things. IEEE Access, 2022, 10, 1688-1705.	4.2	14

#	Article	IF	Citations
19	A system-level approach to adaptivity and fault-tolerance in NoC-based MPSoCs: The MADNESS project. Microprocessors and Microsystems, 2013, 37, 515-529.	2.8	13
20	Curbing the roofline. , 2016, , .		12
21	Enabling Fast ASIP Design Space Exploration: An FPGA-Based Runtime Reconfigurable Prototyper. VLSI Design, 2012, 2012, 1-16.	0.5	10
22	A runtime-adaptive cognitive IoT node for healthcare monitoring. , 2019, , .		10
23	Optimization and deployment of CNNs at the edge. , 2019, , .		10
24	Area and Power Modeling Methodologies for Networks-on-Chip. , 2006, , .		9
25	ASAM: Automatic Architecture Synthesis and Application Mapping. , 2012, , .		8
26	A Custom MPSoC Architecture With Integrated Power Management for Real-Time Neural Signal Decoding. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2014, 4, 230-241.	3.6	8
27	Power and clock gating modelling in coarse grained reconfigurable systems. , 2016, , .		8
28	ALOHA: A Unified Platform-Aware Evaluation Method for CNNs Execution on Heterogeneous Systems at the Edge. IEEE Access, 2021, 9, 133289-133308.	4.2	7
29	Routing Aware Switch Hardware Customization for Networks on Chips. , 2006, , .		6
30	CNN hardware acceleration on a low-power and low-cost APSoC. , 2019, , .		6
31	Runtime Energy versus Quality Tuning in Motion Compensation Filters for HEVC. IFAC-PapersOnLine, 2016, 49, 145-152.	0.9	5
32	On-FPGA real-time processing of biological signals from high-density MEAs: a design space exploration. , 2017, , .		5
33	Exploring NEURAghe: A Customizable Template for APSoC-Based CNN Inference at the Edge. IEEE Embedded Systems Letters, 2020, 12, 62-65.	1.9	5
34	ZyON: Enabling Spike Sorting on APSoC-Based Signal Processors for High-Density Microelectrode Arrays. IEEE Access, 2020, 8, 218145-218160.	4.2	5
35	MPSoCs for real-time neural signal decoding: A low-power ASIP-based implementation. Microprocessors and Microsystems, 2016, 43, 67-80.	2.8	4
36	Modelling and Automated Implementation of Optimal Power Saving Strategies in Coarse-Grained Reconfigurable Architectures. Journal of Electrical and Computer Engineering, 2016, 2016, 1-27.	0.9	3

#	Article	IF	Citations
37	Exploiting FPGAs for technology-aware system-level evaluation of multi-core architectures. , 2010, , .		2
38	Exploiting binary translation for fast ASIP design space exploration on FPGAs. , 2012, , .		2
39	Exploring custom heterogeneous MPSoCs for real-time neural signal decoding. , 2015, , .		2
40	Dataflow-Based Design of Coarse-Grained Reconfigurable Platforms. , 2016, , .		2
41	Real-Time neural signal decoding on heterogeneous MPSocs based on VLIW ASIPs. Journal of Systems Architecture, 2017, 76, 89-101.	4.3	2
42	Runtime Adaptive IoMT Node on Multi-Core Processor Platform. Electronics (Switzerland), 2021, 10, 2572.	3.1	2
43	Designing Routing and Message-Dependent Deadlock Free Networks on Chips. , 2008, , 337-355.		2
44	Target-Aware Neural Architecture Search and Deployment for Keyword Spotting. IEEE Access, 2022, 10, 40687-40700.	4.2	2
45	On the impact of serialization on the cache performances in Network-on-Chip based MPSoCs. , 2007, , .		1
46	Enabling fast Network-on-Chip topology selection: an FPGA-based runtime reconfigurable prototyper. , 2010, , .		1
47	Combining on-hardware prototyping and high-level simulation for DSE of multi-ASIP systems. , 2012, , .		1
48	Towards Self-Adaptive KPN Applications on NoC-Based MPSoCs. Advances in Software Engineering, 2012, 2012, 1-16.	0.6	1
49	A Stream Buffer Mechanism for Pervasive Splitting Transformations on Polyhedral Process Networks. , 2014, , .		1
50	Power modelling for saving strategies in coarse grained reconfigurable systems. , 2015, , .		1
51	Feasibility study of real-time spiking neural network simulations on a swarm intelligence based digital architecture. , 2017, , .		1
52	Architecture-aware design and implementation of CNN algorithms for embedded inference: the ALOHA project. , 2018, , .		1
53	A Closed-Loop System Processing High-Density Electrical Recordings and Visual Stimuli to Study Retinal Circuits Properties. , 2019, , .		1
54	Task-Specific Automation in Deep Learning Processes. Communications in Computer and Information Science, 2021, , 159-169.	0.5	1

#	Article	IF	Citations
55	Optimizing the serialization factor in Networks-on-Chip: a case of study. , 2007, , .		0
56	Online process transformation for polyhedral process networks in shared-memory MPSoCs. , 2014, , .		0
57	A Custom dual-processor System for Real-time Neural Signal Processing. IFAC-PapersOnLine, 2016, 49, 61-67.	0.9	0