Kevin Skadron

List of Publications by Year
in descending order

155 papers	10,866 citations	257450 24 h-index	128289 60 g-index
159 all docs	159 docs citations	159 times ranked	5625 citing authors

#	Article	IF	Citations
1	Supporting Moderate Data Dependency, Position Dependency, and Divergence in PIM-based Accelerators. IEEE Micro, 2022, , 1-1.	1.8	0
2	Synthesizing Legacy String Code for FPGAs Using Bounded Automata Learning. IEEE Micro, 2022, 42, 70-77.	1.8	0
3	PiMulator: a Fast and Flexible Processing-in-Memory Emulation Platform. , 2022, , .		7
4	Gearbox. , 2022, , .		4
5	NOSTalgy: Near-Optimum Run-Time STT-MRAM Quality-Energy Knob Management for Approximate Computing Applications. IEEE Transactions on Computers, 2021, 70, 414-427.	3.4	6
6	BigMap: Future-proofing Fuzzers with Efficient Large Maps. , 2021, , .		1
7	Sieve: Scalable In-situ DRAM-based Accelerator Designs for Massively Parallel k-mer Matching. , 2021, , .		10
8	Sunder: Enabling Low-Overhead and Scalable Near-Data Pattern Matching Acceleration. , 2021, , .		5
9	Edge Crypt-Pi: Securing Internet of Things with Light and Fast Crypto-Processor. Advances in Intelligent Systems and Computing, 2021, , 749-761.	0.6	0
10	Enabling In-SRAM Pattern Processing With Low-Overhead Reporting Architecture. IEEE Computer Architecture Letters, 2020, 19, 167-170.	1.5	2
11	Grapefruit: An Open-Source, Full-Stack, and Customizable Automata Processing on FPGAs. , 2020, , .		18
12	Fulcrum: A Simplified Control and Access Mechanism Toward Flexible and Practical In-Situ Accelerators. , 2020, , .		17
13	FlexAmata: A Universal and Efficient Adaption of Applications to Spatial Automata Processing Accelerators. , 2020, , .		15
14	Impala: Algorithm/Architecture Co-Design for In-Memory Multi-Stride Pattern Matching. , 2020, , .		25
15	ROCKY: A Robust Hybrid On-chip Memory Kit For The Processors With STT-MRAM Cache Technology. IEEE Transactions on Computers, 2020, , 1-1.	3.4	5
16	Towards on-node Machine Learning for Ultra-low-power Sensors Using Asynchronous Î£ Î” Streams. ACM Journal on Emerging Technologies in Computing Systems, 2020, 16, 1-20.	2.3	4
17	Hopscotch. , 2019, , .		9
18	eAP. , 2019, , .		20

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19	GraphTinker: A High Performance Data Structure for Dynamic Graph Processing. , 2019, , .		10
20	Cross-Layer Resilience. , 2019, , .		5
21	Debugging Support for Pattern-Matching Languages and Accelerators. , 2019, , .		6
22	Automata Processing in Reconfigurable Architectures. ACM Transactions on Reconfigurable Technology and Systems, 2019, 12, 1-25.	2.5	7
23	A Scalable and Efficient In-Memory Interconnect Architecture for Automata Processing. IEEE Computer Architecture Letters, 2019, 18, 87-90.	1.5	10
24	Portable Programming with RAPID. IEEE Transactions on Parallel and Distributed Systems, 2019, 30, 939-952.	5.6	2
25	MTTF Enhancement Power-C4 Bump Placement Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1633-1639.	3.1	2
26	Reco-Pi: A reconfigurable Cryptoprocessor for Ï€-Cipher. Journal of Parallel and Distributed Computing, 2019, 133, 420-431.	4.1	2
27	Searching for Potential gRNA Off-Target Sites for CRISPR/Cas9 Using Automata Processing Across Different Platforms. , 2018, , .		22
28	Characterizing and Mitigating Output Reporting Bottlenecks in Spatial Automata Processing Architectures. , 2018, , .		17
29	Tolerating Soft Errors in Processor Cores Using CLEAR (Cross-Layer Exploration for Architecting) Tj ETQq1 1 0.784314 rgBT /Overlock 1 1839-1852.	2.7	14
30	Hierarchical Pattern Mining with the Automata Processor. International Journal of Parallel Programming, 2018, 46, 376-411.	1.5	4
31	AutomataZoo: A Modern Automata Processing Benchmark Suite. , 2018, , .		15
32	ASPEN: A Scalable In-SRAM Architecture for Pushdown Automata. , 2018, , .		10
33	A Scalable Solution for Rule-Based Part-of-Speech Tagging on Novel Hardware Accelerators. , 2018, , .		18
34	MNCaRT: An Open-Source, Multi-Architecture Automata-Processing Research and Execution Ecosystem. IEEE Computer Architecture Letters, 2018, 17, 84-87.	1.5	17
35	Acceleration of Frequent Itemset Mining on FPGA using SDAccel and Vivado HLS. , 2017, , .		7
36	Automata-to-Routing: An Open-Source Toolchain for Design-Space Exploration of Spatial Automata Processing Architectures. , 2017, , .		7

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37	Frequent subtree mining on the automata processor. , 2017, , .		17
38	Dual-Data Rate Transpose-Memory Architecture Improves the Performance, Power and Area of Signal-Processing Systems. Journal of Signal Processing Systems, 2017, 88, 167-184.	2.1	3
39	Cross-Layer Resilience in Low-Voltage Digital Systems: Key Insights. , 2017, , .		3
40	Pre-RTL Voltage and Power Optimization for Low-Cost, Thermally Challenged Multicore Chips. , 2017, , .		5
41	Very Low Voltage (VLV) Design. , 2017, , .		5
42	Classifying images in a histopathological dataset using the cumulative distribution transform on an automata architecture. , 2017, , .		2
43	REAPR: Reconfigurable engine for automata processing. , 2017, , .		23
44	PPE-ARX: Area- and power-efficient VLIW programmable processing element for IoT crypto-systems. , 2017, , .		2
45	Accelerating Weeder: A DNA Motif Search Tool Using the Micron Automata Processor and FPGA. IEICE Transactions on Information and Systems, 2017, E100.D, 2470-2477.	0.7	3
46	Lumos+: Rapid, pre-RTL design space exploration on accelerator-rich heterogeneous architectures with reconfigurable logic. , 2016, , .		2
47	Generating efficient and high-quality pseudo-random behavior on Automata Processors. , 2016, , .		8
48	Feature extraction and image retrieval on an automata structure. , 2016, , .		2
49	A 16-Bit Reconfigurable Encryption Processor for p-Cipher. , 2016, , .		3
50	CLEAR. , 2016, , .		45
51	Closing the power delivery/heat removal cycle for heterogeneous multi-scale systems. , 2016, , .		1
52	An overview of micron's automata processor. , 2016, , .		18
53	ANMLzoo: a benchmark suite for exploring bottlenecks in automata processing engines and architectures. , 2016, , .		48
54	Entity resolution acceleration using the automata processor. , 2016, , .		21

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55	Sequential pattern mining with the Micron automata processor. , 2016, , .		32
56	Near-Memory Data Services. IEEE Micro, 2016, 36, 6-13.	1.8	11
57	Tolerating the Consequences of Multiple EM-Induced C4 Bump Failures. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2335-2344.	3.1	5
58	RAPID Programming of Pattern-Recognition Processors. , 2016, , .		14
59	RAPID Programming of Pattern-Recognition Processors. ACM SIGPLAN Notices, 2016, 51, 593-605.	0.2	2
60	RAPID Programming of Pattern-Recognition Processors. Operating Systems Review (ACM), 2016, 50, 593-605.	1.9	3
61	RAPID Programming of Pattern-Recognition Processors. Computer Architecture News, 2016, 44, 593-605.	2.5	1
62	SPEC ACCEL: A Standard Application Suite for Measuring Hardware Accelerator Performance. Lecture Notes in Computer Science, 2015, , 46-67.	1.3	24
63	Transient voltage noise in charge-recycled power delivery networks for many-layer 3D-IC. , 2015, , .		7
64	Regular expression acceleration on the micron automata processor: Brill tagging as a case study. , 2015, , .		12
65	Power-efficient embedded processing with resilience and real-time constraints. , 2015, , .		6
66	A cross-layer design exploration of charge-recycled power-delivery in many-layer 3d-IC. , 2015, , .		6
67	Yield-aware Performance-Cost Characterization for Multi-Core SIMT. , 2015, , .		5
68	Association Rule Mining with the Micron Automata Processor. , 2015, , .		51
69	Brill tagging on the Micron Automata Processor. , 2015, , .		31
70	A meta-algorithm for classification by feature nomination. , 2014, , .		2
71	Walking Pads. , 2014, , .		12
72	BenchFriend. International Journal of High Performance Computing Applications, 2014, 28, 238-250.	3.7	18

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73	Walking pads: Fast power-supply pad-placement optimization. , 2014, , .		7
74	The resilience wall: Cross-layer solution strategies. , 2014, , .		12
75	Architecture implications of pads as a scarce resource. , 2014, , .		34
76	Real-world design and evaluation of compiler-managed GPU redundant multithreading. , 2014, , .		44
77	Real-world design and evaluation of compiler-managed GPU redundant multithreading. Computer Architecture News, 2014, 42, 73-84.	2.5	17
78	Architecture implications of pads as a scarce resource. Computer Architecture News, 2014, 42, 373-384.	2.5	13
79	Dymaxion++: A Directive-Based API to Optimize Data Layout and Memory Mapping for Heterogeneous Systems. , 2014, , .		4
80	Image classification by multi-kernel dictionary learning. , 2014, , .		3
81	Evaluating Overheads of Multibit Soft-Error Protection in the Processor Core. IEEE Micro, 2013, 33, 56-65.	1.8	15
82	Implications of the Power Wall: Dim Cores and Reconfigurable Logic. IEEE Micro, 2013, 33, 40-48.	1.8	33
83	Pannotia: Understanding irregular GPGPU graph applications. , 2013, , .		119
84	Architectural implications of spatial thermal filtering. The Integration VLSI Journal, 2013, 46, 44-56.	2.1	3
85	Binary Interval Search: a scalable algorithm for counting interval intersections. Bioinformatics, 2013, 29, 1-7.	4.1	58
86	Trellis: Portability across architectures with a high-level framework. Journal of Parallel and Distributed Computing, 2013, 73, 1400-1413.	4.1	6
87	Introducing the New Editor-in-Chief of the IEEE Computer Architecture Letters. IEEE Computer Architecture Letters, 2013, 12, 1-1.	1.5	0
88	Robust SIMD: Dynamically Adapted SIMD Width and Multi-Threading Depth. , 2012, , .		15
89	A Hierarchical Thread Scheduler and Register File for Energy-Efficient Throughput Processors. ACM Transactions on Computer Systems, 2012, 30, 1-38.	0.8	30
90	Recent thermal management techniques for microprocessors. ACM Computing Surveys, 2012, 44, 1-42.	23.0	167

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91	ArchFP: Rapid prototyping of pre-RTL floorplans. , 2012, , .		4
92	Increasing Utilization in Modern Warehouse-Scale Computers Using Bubble-Up. IEEE Micro, 2012, 32, 88-99.	1.8	38
93	ArchFP: Rapid prototyping of pre-RTL floorplans. , 2012, , .		10
94	Using cycle stacks to understand scaling bottlenecks in multi-threaded workloads. , 2011, , .		31
95	A reconfigurable simulator for large-scale heterogeneous multicore architectures. , 2011, , .		5
96	Thermal benefit of multi-core floorplanning: A limits study. Sustainable Computing: Informatics and Systems, 2011, 1, 286-293.	2.2	2
97	Editorial: Letter from the Editor-in-Chief. IEEE Computer Architecture Letters, 2011, 10, 1-3.	1.5	1
98	Scaling with Design Constraints: Predicting the Future of Big Chips. IEEE Micro, 2011, 31, 16-29.	1.8	100
99	Temperature-Aware Architecture: Lessons and Opportunities. IEEE Micro, 2011, 31, 82-86.	1.8	19
100	A Performance Study for Iterative Stencil Loops on GPUs with Ghost Zone Optimizations. International Journal of Parallel Programming, 2011, 39, 115-142.	1.5	37
101	Dymaxion. , 2011, , .		80
102	Cost-effective safety and fault localization using distributed temporal redundancy. , 2011, , .		13
103	Energy-efficient mechanisms for managing thread context in throughput processors. Computer Architecture News, 2011, 39, 235-246.	2.5	29
104	Dynamic warp subdivision for integrated branch and memory divergence tolerance. Computer Architecture News, 2010, 38, 235-246.	2.5	39
105	Editorial: Letter from the Editor-in-Chief. IEEE Computer Architecture Letters, 2010, 9, 37-44.	1.5	0
106	Federation. Transactions on Architecture and Code Optimization, 2010, 7, 1-38.	2.0	13
107	Dynamic warp subdivision for integrated branch and memory divergence tolerance. , 2010, , .		166
108	Predictive Temperature-Aware DVFS. IEEE Transactions on Computers, 2010, 59, 127-133.	3.4	78

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109	Accelerating SQL database operations on a GPU with CUDA. , 2010, , .		181
110	Interaction of scaling trends in processor architecture and cooling. , 2010, , .		19
111	The Sharing Tracker: Using Ideas from Cache Coherence Hardware to Reduce Off-Chip Memory Traffic with Non-Coherent Caches. , 2010, , .		20
112	Exploiting inter-thread temporal locality for chip multithreading. , 2010, , .		14
113	Exploring the thermal impact on manycore processor performance. , 2010, , .		11
114	A characterization of the Rodinia benchmark suite with comparison to contemporary CMP workloads. , 2010, , .		211
115	Temperature-to-power mapping. , 2010, , .		18
116	Thermal Modeling for Processors and Systems-on-Chip. , 2010, , 243-257.		0
117	Accelerating leukocyte tracking using CUDA: A case study in leveraging manycore coprocessors. , 2009, , .		45
118	Performance modeling and automatic ghost zone optimization for iterative stencil loops on GPUs. , 2009, , .		103
119	Increasing memory miss tolerance for SIMD cores. , 2009, , .		47
120	Rodinia: A benchmark suite for heterogeneous computing. , 2009, , .		2,150
121	Differentiating the roles of IR measurement and simulation for power and temperature-aware design. , 2009, , .		42
122	Avoiding cache thrashing due to private data placement in last-level cache for manycore scaling. , 2009, , .		21
123	A performance study of general-purpose applications on graphics processors using CUDA. Journal of Parallel and Distributed Computing, 2008, 68, 1370-1380.	4.1	496
124	Scalable Parallel Programming with CUDA. Queue, 2008, 6, 40-53.	1.1	1,344
125	On-Demand Solution to Minimize I-Cache Leakage Energy with Maintaining Performance. IEEE Transactions on Computers, 2008, 57, 7-24.	3.4	11
126	Accurate, Pre-RTL Temperature-Aware Design Using a Parameterized, Geometric Thermal Model. IEEE Transactions on Computers, 2008, 57, 1277-1288.	3.4	92

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127	Accelerating Compute-Intensive Applications with GPUs and FPGAs. , 2008, , .		212
128	Federation. , 2008, , .		34
129	Many-core design from a thermal perspective. , 2008, , .		79
130	Multi-mode energy management for multi-tier server clusters. , 2008, , .		92
131	Predictive design space exploration using genetically programmed response surfaces. , 2008, , .		26
132	Enhancing Energy Efficiency in Multi-tier Web Server Clusters via Prioritization. , 2007, , .		13
133	Impact of Process Variations on Multicore Performance Symmetry. , 2007, , .		89
134	Low-Power Design and Temperature Management. IEEE Micro, 2007, 27, 46-57.	1.8	1
135	Dynamic Voltage Scaling in Multitier Web Servers with End-to-End Delay Control. IEEE Transactions on Computers, 2007, 56, 444-458.	3.4	219
136	Interconnect Lifetime Prediction for Reliability-Aware Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 159-172.	3.1	38
137	Small-scale reconfigurability for improved performance and double-precision in graphics hardware. International Journal of Electronics, 2007, 94, 549-561.	1.4	0
138	HotSpot: a compact thermal modeling methodology for early-stage VLSI design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 501-513.	3.1	860
139	Design and Implementation of an Energy Efficient Multimedia Playback System. , 2006, , .		1
140	A Novel Software Solution for Localized Thermal Problems. Lecture Notes in Computer Science, 2006, , 63-74.	1.3	10
141	The visual vulnerability spectrum. , 2006, , .		19
142	Accelerated warmup for sampled microarchitecture simulation. Transactions on Architecture and Code Optimization, 2005, 2, 78-108.	2.0	17
143	Improved Thermal Management with Reliability Banking. IEEE Micro, 2005, 25, 40-49.	1.8	29
144	Understanding the energy efficiency of simultaneous multithreading. , 2004, , .		25

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145	Compact thermal modeling for temperature-aware design. , 2004, , .		191
146	Temperature-aware microarchitecture. Transactions on Architecture and Code Optimization, 2004, 1, 94-125.	2.0	640
147	Power-aware branch prediction: characterization and design. IEEE Transactions on Computers, 2004, 53, 168-186.	3.4	39
148	Alloyed Branch History: Combining Global and Local Branch History for Robust Performance. International Journal of Parallel Programming, 2003, 31, 137-177.	1.5	8
149	Power-aware computing. Computer, 2003, 36, 35-38.	1.1	49
150	HotSpot: a dynamic compact thermal model at the processor-architecture level. Microelectronics Journal, 2003, 34, 1153-1165.	2.0	88
151	Temperature-aware microarchitecture. , 2003, , .		695
152	Temperature-aware computer systems: opportunities and challenges. IEEE Micro, 2003, 23, 52-61.	1.8	99
153	Temperature-aware microarchitecture. Computer Architecture News, 2003, 31, 2-13.	2.5	275
154	Control-theoretic dynamic frequency and voltage scaling for multimedia workloads. , 2002, , .		83
155	Branch prediction, instruction-window size, and cache size: performance trade-offs and simulation techniques. IEEE Transactions on Computers, 1999, 48, 1260-1281.	3.4	75