Leonel Sousa

List of Publications by Year
in descending order

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274	3,504	172386	233338
papers	citations	29	45
		h-index	g-index

288	288	288	2429
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Inter-Algorithm Multiobjective Cooperation for Phylogenetic Reconstruction on Amino Acid Data. IEEE Transactions on Cybernetics, 2022, 52, 3577-3591.	6.2	1
2	Exploiting multi-level parallel metaheuristics and heterogeneous computing to boost phylogenetics. Future Generation Computer Systems, 2022, 127, 208-224.	4.9	2
3	Uncertainty Estimation via Monte Carlo Dropout in CNN-Based mmWave MIMO Localization. IEEE Signal Processing Letters, 2022, 29, 269-273.	2.1	4
4	Modeling and evaluation of dispatching policies in IaaS cloud data centers using SANs. Sustainable Computing: Informatics and Systems, 2022, 33, 100617.	1.6	0
5	A genetic-based approach for service placement in fog computing. Journal of Supercomputing, 2022, 78, 10854-10875.	2.4	11
6	NTT Architecture for a Linux-Ready RISC-V Fully-Homomorphic Encryption Accelerator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2669-2682.	3.5	14
7	Nonconventional Computer Arithmetic Circuits, Systems and Applications. IEEE Circuits and Systems Magazine, 2021, 21, 6-40.	2.6	27
8	Modeling Epidemic Routing: Capturing Frequently Visited Locations While Preserving Scalability. IEEE Transactions on Vehicular Technology, 2021, 70, 2713-2727.	3.9	5
9	Variable Latency Carry Speculative Adders with Input-based Dynamic Configuration. Computers and Electrical Engineering, 2021, 93, 107247.	3.0	3
10	Number Theoretic Transform Architecture suitable to Lattice-based Fully-Homomorphic Encryption. , 2021, , .		3
11	Retargeting Tensor Accelerators for Epistasis Detection. IEEE Transactions on Parallel and Distributed Systems, 2021, 32, 2160-2174.	4.0	10
12	Mansard Roofline Model: Reinforcing the Accuracy of the Roofs. ACM Transactions on Modeling and Performance Evaluation of Computing Systems, 2021, 6, 1-23.	0.8	2
13	Fourth-Order Exhaustive Epistasis Detection for the xPU Era. , 2021, , .		2
14	Editorial on the Special Section on Algorithms, Circuits, and Systems for Signal Processing at the Edge. IEEE Open Journal of Circuits and Systems, 2021, 2, 766-768.	1.4	0
15	Modeling and Evaluation of Service Composition in Commercial Multiclouds Using Timed Colored Petri Nets. IEEE Transactions on Systems, Man, and Cybernetics: Systems, 2020, 50, 947-961.	5.9	12
16	Parallelism exploration for 3D high-efficiency video coding depth modeling mode one. Journal of Real-Time Image Processing, 2020, 17, 787-797.	2.2	3
17	Deep Learning Architectures for Accurate Millimeter Wave Positioning in 5G. Neural Processing Letters, 2020, 51, 487-514.	2.0	35
18	Parallel evolutionary computation for multiobjective gene interaction analysis. Journal of Computational Science, 2020, 40, 101068.	1.5	2

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19	Towards the Integration of Reverse Converters into the RNS Channels. IEEE Transactions on Computers, 2020, 69, 342-348.	2.4	4
20	Multicore Parallelism Exploration Targeting 3D-HEVC Intra-Frame Prediction. IEEE Design and Test, 2020, 37, 15-21.	1.1	0
21	Exploring the Binary Precision Capabilities of Tensor Cores for Epistasis Detection. , 2020, , .		8
22	An asymptotically faster version of FV supported on HPR. , 2020, , .		0
23	Raising the Abstraction Level of a Deep Learning Design on FPGAs. IEEE Access, 2020, 8, 205148-205161.	2.6	4
24	Dethroning GPS: Low-Power Accurate 5G Positioning Systems Using Machine Learning. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 240-252.	2.7	32
25	A hybrid algorithm for task scheduling on heterogeneous multiprocessor embedded systems. Applied Soft Computing Journal, 2020, 91, 106202.	4.1	20
26	Improving the Efficiency of SVM Classification With FHE. IEEE Transactions on Information Forensics and Security, 2020, 15, 1709-1722.	4.5	13
27	Temperatureâ€aware core management in MPSoCs: modelling and evaluation using MRMs. IET Computers and Digital Techniques, 2020, 14, 17-26.	0.9	1
28	Application-driven Cache-Aware Roofline Model. Future Generation Computer Systems, 2020, 107, 257-273.	4.9	8
29	GPU acceleration of Fitchâ€™s parsimony on protein data: from Kepler to Turing. Journal of Supercomputing, 2020, 76, 9827-9853.	2.4	1
30	The Role of Non-Positional Arithmetic on Efficient Emerging Cryptographic Algorithms. IEEE Access, 2020, 8, 59533-59549.	2.6	7
31	A Lattice-Based Enhanced Privacy ID. Lecture Notes in Computer Science, 2020, , 15-31.	1.0	2
32	Accelerating 3-Way Epistasis Detection with CPU+GPU Processing. Lecture Notes in Computer Science, 2020, , 106-126.	1.0	7
33	Software Emulation of Quantum Resistant Trusted Platform Modules. , 2020, , .		0
34	Efficient Modular Adder Designs Based on Thermometer and One-Hot Coding. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2142-2155.	2.1	20
35	Enhancing Beamformed Fingerprint Outdoor Positioning with Hierarchical Convolutional Neural Networks. , 2019, , .		6
36	Scalable Performance Analysis of Epidemic Routing Considering Skewed Location Visiting Preferences. , 2019, , .		3

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37	On the Design of RNS Inter-Modulo Processing Units for the Arithmetic-Friendly Moduli Sets {2n+k, 2nâ^' 1, 2n+1 â^' 1}. Computer Journal, 2019, 62, 292-300.	1.5	11
38	A methodical FHE-based cloud computing model. Future Generation Computer Systems, 2019, 95, 639-648.	4.9	5
39	Comparative assessment of GPGPU technologies to accelerate objective functions: A case study on parsimony. Journal of Parallel and Distributed Computing, 2019, 126, 67-81.	2.7	4
40	More efficient, provably-secure direct anonymous attestation from lattices. Future Generation Computer Systems, 2019, 99, 425-458.	4.9	9
41	A multiobjective adaptive approach for the inference of evolutionary relationships in protein-based scenarios. Information Sciences, 2019, 485, 281-300.	4.0	5
42	HyPoRes: An Hybrid Representation System for ECC. , 2019, , .		2
43	New energyâ€efficient hybrid wideâ€operand adder architecture. IET Circuits, Devices and Systems, 2019, 13, 1221-1231.	0.9	17
44	Sign Identifier for the Enhanced Three Moduli Set {2n + k, 2n â^'â€‰1, 2n+â€‰1 â^'â€‰1}. Journal of Signal Processing Systems, 2019, 91, 953-961.	1.4	7
45	Modeling Non-Uniform Memory Access on Large Compute Nodes with the Cache-Aware Roofline Model. IEEE Transactions on Parallel and Distributed Systems, 2019, 30, 1374-1389.	4.0	11
46	Analysis of MOEA/D Approaches for Inferring Ancestral Relationships. Lecture Notes in Computer Science, 2019, , 168-180.	1.0	0
47	Temperature-aware dynamic voltage and frequency scaling enabled MPSoC modeling using Stochastic Activity Networks. Microprocessors and Microsystems, 2018, 60, 15-23.	1.8	6
48	Highly parallel HEVC decoding for heterogeneous systems with CPU and GPU. Signal Processing: Image Communication, 2018, 62, 93-105.	1.8	5
49	A Survey on Fully Homomorphic Encryption. ACM Computing Surveys, 2018, 50, 1-33.	16.1	82
50	Towards Efficient Modular Adders based on Reversible Circuits. , 2018, , .		9
51	MrBayes sMC3. International Journal of High Performance Computing Applications, 2018, 32, 246-265.	2.4	4
52	Beamformed Fingerprint Learning for Accurate Millimeter Wave Positioning. , 2018, , .		16
53	Accelerating CNN computation. , 2018, , .		0
54	Cache-Aware Roofline Model and Medical Image Processing Optimizations in GPUs. Lecture Notes in Computer Science, 2018, , 509-526.	1.0	0

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55	Phylogenetic Reconstructions Using an Indicator-Based Bat Algorithm for Multicore Processors. , 2018, , .		0
56	3D-HEVC DMM-1 Parallelism Exploration Targeting Multicore Systems. , 2018, , .		3
57	Implementation Strategy of Convolution Neural Networks on Field Programmable Gate Arrays for Appliance Classification Using the Voltage and Current (V-I) Trajectory. Energies, 2018, 11, 2460.	1.6	30
58	Analysis of Scheduling Policies in Metaheuristics for Evolutionary Biology. , 2018, , .		0
59	Data-Aided Fast Beamforming Selection for 5G. , 2018, , .		10
60	Performability-Based Workflow Scheduling in Grids. Computer Journal, 2018, 61, 1479-1495.	1.5	7
61	Multiobjective Frog-Leaping Optimization for the Study of Ancestral Relationships in Protein Data. IEEE Transactions on Evolutionary Computation, 2018, 22, 879-893.	7.5	8
62	Modeling Large Compute Nodes withÂHeterogeneous Memories withÂCache-Aware Roofline Model. Lecture Notes in Computer Science, 2018, , 91-113.	1.0	4
63	Efficient Reductions in Cyclotomic Rings - Application to Ring-LWE Based FHE Schemes. Lecture Notes in Computer Science, 2018, , 151-171.	1.0	2
64	Beyond the Roofline: Cache-Aware Power and Energy-Efficiency Modeling for Multi-Cores. IEEE Transactions on Computers, 2017, 66, 52-58.	2.4	13
65	An Efficient Component for Designing Signed Reverse Converters for a Class of RNS Moduli Sets of Composite Form ${2^{k}, 2^{P}-1}$. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 48-59.	2.1	8
66	Sign Detection and Number Comparison on RNS 3-Moduli Sets $${2^n-1, 2^{n+x}, 2^n+1}$$ { 2 n - 1 , 2 n + x , 2 n + 1 }. Circuits, Systems, and Signal Processing, 2017, 36, 1224-1246.	1.2	17
67	GPU Parallelization of HEVC In-Loop Filters. International Journal of Parallel Programming, 2017, 45, 1515-1535.	1.1	3
68	Energyâ€aware mechanism for stencilâ€based MPDATA algorithm with constraints. Concurrency Computation Practice and Experience, 2017, 29, e4016.	1.4	10
69	TrustZone-backed bitcoin wallet. , 2017, , .		23
70	Performance and power modeling and evaluation of virtualized servers in IaaS clouds. Information Sciences, 2017, 394-395, 106-122.	4.0	31
71	Arithmetical Improvement of the Round-Off for Cryptosystems in High-Dimensional Lattices. IEEE Transactions on Computers, 2017, 66, 2005-2018.	2.4	4
72	Special issue on real-time energy-aware circuits and systems for HEVC and for its 3D and SVC extensions. Journal of Real-Time Image Processing, 2017, 13, 1-3.	2.2	6

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73	On Boosting Energy-Efficiency of Heterogeneous Embedded Systems via Game Theory. , 2017, , .		1
74	Accelerating the phylogenetic parsimony function on heterogeneous systems. Concurrency Computation Practice and Experience, 2017, 29, e4046.	1.4	3
75	Introduction to Residue Number System: Structure and Teaching Methodology. , 2017, , 3-17.		3
76	RNS-Based Embedded Processor Design. , 2017, , 19-47.		0
77	GHEVC: An Efficient HEVC Decoder for Graphics Processing Units. IEEE Transactions on Multimedia, 2017, 19, 459-474.	5.2	21
78	Design Space Exploration of LDPC Decoders Using High-Level Synthesis. IEEE Access, 2017, 5, 14600-14615.	2.6	18
79	Exploring GPU performance, power and energy-efficiency bounds with Cache-aware Roofline Modeling. , 2017, , .		28
80	A Reduced-Bias Approach With a Lightweight Hard-Multiple Generator to Design a Radix-8 Modulo $2^{n} + 1$ Multiplier. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 817-821.	2.2	7
81	A stochastic number representation for fully homomorphic cryptography. , 2017, , .		2
82	Performance Analysis with Cache-Aware Roofline Model in Intel Advisor. , 2017, , .		14
83	Analyzing Performance of Multi-cores and Applications with Cache-aware Roofline Model. , 2017, , .		0
84	A Multifunctional Unit for Designing Efficient RNS-Based Datapaths. IEEE Access, 2017, 5, 25972-25986.	2.6	12
85	Enhancing Data Parallelism of Fully Homomorphic Encryption. Lecture Notes in Computer Science, 2017, , 194-207.	1.0	4
86	Exploiting task and data parallelism for advanced video coding on hybrid CPUÂ+ÂGPU platforms. Journal of Real-Time Image Processing, 2016, 11, 571-587.	2.2	9
87	High-Level Designs of Complex FIR Filters on FPGAs for the SKA. , 2016, , .		7
88	Efficient HEVC decoder for heterogeneous CPU with GPU systems. , 2016, , .		2
89	Area-delay-power-aware adder placement method for RNS reverse converter design. , 2016, , .		0
90	A Survey on Programmable LDPC Decoders. IEEE Access, 2016, 4, 6704-6718.	2.6	19

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91	Combining Residue Arithmetic to Design Efficient Cryptographic Circuits and Systems. IEEE Circuits and Systems Magazine, 2016, 16, 6-32.	2.6	43
92	Ubiquitous Multimedia: Emerging Research on Multimedia Computing. IEEE MultiMedia, 2016, 23, 12-15.	1.5	8
93	Adaptive Scheduling Framework for Real-Time Video Encoding on Heterogeneous Systems. IEEE Transactions on Circuits and Systems for Video Technology, 2016, 26, 597-611.	5.6	6
94	A Framework for Application-Guided Task Management on Heterogeneous Embedded Systems. Transactions on Architecture and Code Optimization, 2016, 12, 1-25.	1.6	12
95	Method for designing two levels RNS reverse converters for large dynamic ranges. The Integration VLSI Journal, 2016, 55, 22-29.	1.3	2
96	GPU-assisted HEVC intra decoder. Journal of Real-Time Image Processing, 2016, 12, 531-547.	2.2	10
97	Run-Time Machine Learning for HEVC/H.265 Fast Partitioning Decision. , 2015, , .		9
98	Featuring Immediate Revocation in Mikey-Sakke (FIRM). , 2015, , .		0
99	GPU acceleration of the HEVC decoder inter prediction module. , 2015, , .		3
100	Accelerating Phylogenetic Inference on Heterogeneous OpenCL Platforms. , 2015, , .		0
101	High performance IP core for HEVC quantization. , 2015, , .		4
102	HEVC in-loop filters GPU parallelization in embedded systems. , 2015, , .		12
103	Novel methodology to improve Multi-moduli architectures for Binary-to-RNS conversion. , 2015, , .		0
104	<inline-formula><tex-math>2^n</tex-math><alternatives> <inline-graphic xlink:type="simple" xlink:href="sousa-ieq1-2401026.gif"/></alternatives></inline-formula> RNS Scalers for Extended 4-Moduli Sets. IEEE Transactions on Computers, 2015, 64, 3322-3334.	2.4	24
105	Stretching the limits of Programmable Embedded Devices for Public-key Cryptography. , 2015, , .		4
106	Towards GPU HEVC intra decoding: Seizing fine-grain parallelism. , 2015, , .		9
107	RNS reverse converters based on the new Chinese Remainder Theorem I. , 2015, , .		1
108	Base Transformation With Injective Residue Mapping for Dynamic Range Reduction in RNS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2248-2259.	3.5	5

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109	Programmable RNS lattice-based parallel cryptographic decryption. , 2015, , .		8
110	Arithmetic-Based Binary-to-RNS Converter Modulo <inline-formula> <tex-math notation="LaTeX">${{2^{n}{pm}k}}$ </tex-math></inline-formula> for <inline-formula> <tex-math notation="LaTeX">jn </tex-math></inline-formula>-bit Dynamic Range. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 603-607.	2.1	14
111	Real-time implementation of remotely sensed hyperspectral image unmixing on GPUs. Journal of Real-Time Image Processing, 2015, 10, 469-483.	2.2	42
112	Reverse Converter Design via Parallel-Prefix Adders: Novel Components, Methodology, and Implementations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 374-378.	2.1	20
113	Collaborative inter-prediction on CPU+GPU systems. , 2014, , .		2
114	ROM-less RNS-to-binary converter moduli {2²ⁿ ࢤ 1, 2²ⁿ + 1, 2ⁿ ࢤ 3, 2ⁿ + 3}. , 2014, , .		1
115	EFFICIENT METHOD FOR DESIGNING MODULO {2n Â± k} MULTIPLIERS. Journal of Circuits, Systems and Computers, 2014, 23, 1450001.	1.0	7
116	Reconfigurable data flow engine for HEVC motion estimation. , 2014, , .		7
117	On the Evaluation of Multi-core Systems with SIMD Engines for Public-Key Cryptography. , 2014, , .		4
118	SchedMon: A Performance and Energy Monitoring Tool for Modern Multi-cores. Lecture Notes in Computer Science, 2014, , 230-241.	1.0	10
119	Cooperative CPU+GPU deblocking filter parallelization for high performance HEVC video codecs. , 2014, , .		14
120	Combining flexibility with low power: Dataflow and wide-pipeline LDPC decoding engines in the Gbit/s era. , 2014, , .		10
121	FEVES: Framework for Efficient Parallel Video Encoding on Heterogeneous Systems. , 2014, , .		2
122	Efficient sign identification engines for integers represented in RNS extended 3â€moduli set {2 ⁿ â^' 1, 2 ⁿ ⁺ ^k , 2 ⁿ + 1}. Electronics Letters, 2014, 50, 1138-1139.	0.5	12
123	Performance-Aware Task Management and Frequency Scaling in Embedded Systems. , 2014, , .		3
124	Cache-aware Roofline model: Upgrading the loft. IEEE Computer Architecture Letters, 2014, 13, 21-24.	1.0	89
125	An Efficient Scalable RNS Architecture for Large Dynamic Ranges. Journal of Signal Processing Systems, 2014, 77, 191-205.	1.4	9
126	Method for Designing Efficient Mixed Radix Multipliers. Circuits, Systems, and Signal Processing, 2014, 33, 3165-3193.	1.2	3

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127	Method for designing multi-channel RNS architectures to prevent power analysis SCA. , 2014, , .		3
128	Dynamic Load Balancing for Real-Time Video Encoding on Heterogeneous CPU+GPU Systems. IEEE Transactions on Multimedia, 2014, 16, 108-121.	5.2	30
129	Unified transform architecture for AVC, AVS, VC-1 and HEVC high-performance codecs. Eurasip Journal on Advances in Signal Processing, 2014, 2014, .	1.0	9
130	A Flexible Architecture for Modular Arithmetic Hardware Accelerators based on RNS. Journal of Signal Processing Systems, 2014, 76, 249-259.	1.4	2
131	Monitoring Performance and Power for Application Characterization with the Cache-Aware Roofline Model. Lecture Notes in Computer Science, 2014, , 747-760.	1.0	6
132	Finite-Difference in Time-Domain Scalable Implementations on CUDA and OpenCL. , 2014, , 223-242.		0
133	A compact and scalable RNS architecture. , 2013, , .		2
134	On the Design of RNS Reverse Converters for the Four-Moduli Set ${f{2^{mmb n}+1, 2^{mmb n}-1, 2^{mmb n}, 2^{{mmb n}+1}+1}}$. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1945-1949.	2.1	24
135	A comparison of computing architectures and parallelization frameworks based on a two-dimensional FDTD. , 2013, , .		2
136	Method to Design General RNS Reverse Converters for Extended Moduli Sets. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 877-881.	2.2	19
137	The CRNS framework and its application to programmable and reconfigurable cryptography. Transactions on Architecture and Code Optimization, 2013, 9, 1-25.	1.6	23
138	DARNS:A randomized multi-modulo RNS architecture for double-and-add in ECC to prevent power analysis side channel attacks. , 2013, , .		2
139	Randomised multiâ€modulo residue number system architecture for doubleâ€andâ€add to prevent power analysis side channel attacks. IET Circuits, Devices and Systems, 2013, 7, 283-293.	0.9	5
140	A Lab Project on the Design and Implementation of Programmable and Configurable Embedded Systems. IEEE Transactions on Education, 2013, 56, 322-328.	2.0	13
141	RNS Reverse Converters for Moduli Sets With Dynamic Ranges up to $(8n+1)$-bit. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 1487-1500.	3.5	41
142	Scalable Unified Transform Architecture for Advanced Video Coding Embedded Systems. International Journal of Parallel Programming, 2013, 41, 236-260.	1.1	1
143	An RNS-based architecture targeting hardware accelerators for modular arithmetic. , 2013, , .		1
144	Open the Gates: Using High-level Synthesis towards programmable LDPC decoders on FPGAs. , 2013, , .		10

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145	Accelerating the Computation of Induced Dipoles for Molecular Mechanics with Dataflow Engines. , 2013, , .		8
146	Multi-level Parallelization of Advanced Video Coding on Hybrid CPU+GPU Platforms. Lecture Notes in Computer Science, 2013, , 165-174.	1.0	6
147	RNS-Based Elliptic Curve Point Multiplication for Massive Parallel Architectures. Computer Journal, 2012, 55, 629-647.	1.5	49
148	Scheduling Divisible Loads on Heterogeneous Desktop Systems with Limited Memory. Lecture Notes in Computer Science, 2012, , 491-501.	1.0	2
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163	Hierarchical Partitioning Algorithm for Scientific Computing on Highly Heterogeneous CPU + GPU Clusters. Lecture Notes in Computer Science, 2012, , 489-501.	1.0	8
164	Binary-to-RNS Conversion Units for moduli {2^n ± 3}. , 2011, , .		8
165	GPU-based DVB-S2 LDPC decoder with high throughput and fast error floor detection. Electronics Letters, 2011, 47, 542.	0.5	23
166	Real-time DVB-S2 LDPC decoding on many-core GPU accelerators. , 2011, , .		7
167	Massively LDPC Decoding on Multicore Architectures. IEEE Transactions on Parallel and Distributed Systems, 2011, 22, 309-322.	4.0	85
168	A flexible architecture for the computation of direct and inverse transforms in H.264/AVC video codecs. IEEE Transactions on Consumer Electronics, 2011, 57, 936-944.	3.0	1
169	Modeling and Evaluating Non-shared Memory CELL/BE Type Multi-core Architectures for Local Image and Video Processing. Journal of Signal Processing Systems, 2011, 62, 301-318.	1.4	2
170	A tutorial overview on the properties of the discrete cosine transform for encoded image and video processing. Signal Processing, 2011, 91, 2443-2464.	2.1	26
171	High throughput and scalable architecture for unified transform coding in embedded H.264/AVC video coding systems. , 2011, , .		2
172	Parallel LDPC Decoding. , 2011, , 619-628.		2
173	Measuring and Extraction of Biological Information on New Handheld Biochip-Based Microsystem. IEEE Transactions on Instrumentation and Measurement, 2010, 59, 56-62.	2.4	2
174	On the Modeling of New Tunnel Junction Magnetoresistive Biosensors. IEEE Transactions on Instrumentation and Measurement, 2010, 59, 92-100.	2.4	7
175	A quantitative analysis of firing rate estimators: Unveiling bias sources. Neurocomputing, 2010, 73, 2944-2954.	3.5	0
176	Challenges and trends in the development of a magnetoresistive biochip portable platform. Journal of Magnetism and Magnetic Materials, 2010, 322, 1655-1663.	1.0	55
177	H.264/AVC framework for multi-core embedded video encoders. , 2010, , .		2
178	Unifying stream based and reconfigurable computing to design application accelerators. , 2010, , .		0
179	Iterative induced dipoles computation for molecular mechanics on GPUs. , 2010, , .		5
180	Programming Cell/BE and GPUs systems for real-time video encoding. Proceedings of SPIE, 2010, , .	0.8	0

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181	p264. , 2010, , .		13
182	Arithmetic Units for RNS Moduli {2n-3} and {2n+3} Operations. , 2010, , .		18
183	Elliptic Curve point multiplication on GPUs. , 2010, , .		30
184	Exploiting SIMD extensions for linear image processing with OpenCL. , 2010, , .		3
185	Collaborative execution environment for heterogeneous parallel systems. , 2010, , .		2
186	Embedded multicore architectures for LDPC decoding. , 2010, , .		2
187	An improved RNS generator 2ⁿ ± k based on threshold logic. , 2010, , .		1
188	Efficient Independent Component Analysis on a GPU. , 2010, , .		10
189	Hardware/software co-design of H.264/AVC encoders for multi-core embedded systems. , 2010, , .		2
190	Fine-grain Parallelism Using Multi-core, Cell/BE, and GPU Systems: Accelerating the Phylogenetic Likelihood Function. , 2009, , .		37
191	Multi-core platforms for signal processing: source and channel coding. , 2009, , .		2
192	On the design of distributed autonomous embedded systems for biomedical applications. , 2009, , .		3
193	A Portable and Autonomous Magnetic Detection Platform for Biosensing. Sensors, 2009, 9, 4119-4137.	2.1	76
194	Neural code metrics: Analysis and application to the assessment of neural models. Neurocomputing, 2009, 72, 2337-2350.	3.5	9
195	A Feature Selection Algorithm for the Regularization of Neuron Models. IEEE Transactions on Instrumentation and Measurement, 2009, 58, 3824-3830.	2.4	2
196	Magnetoresistive biochip-based portable platforms for biomolecular recognition detection. New Biotechnology, 2009, 25, S358-S359.	2.4	0
197	Parallel LDPC Decoding on GPUs Using a Stream-Based Computing Approach. Journal of Computer Science and Technology, 2009, 24, 913-924.	0.9	75
198	Femtomolar limit of detection with a magnetoresistive biochip. Biosensors and Bioelectronics, 2009, 24, 2690-2695.	5.3	107

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199	Development and evaluation of scalable video motion estimators on GPU. , 2009, , .		9
200	Distributed Software Platform for Automation and Control of General Anaesthesia. , 2009, , .		0
201	Compact and Flexible Microcoded Elliptic Curve Processor for Reconfigurable Devices. , 2009, , .		7
202	CaravelaMPI: Message Passing Interface for Parallel GPU-Based Applications. , 2009, , .		5
203	Modelling and programming stream-based distributed computing based on the meta-pipeline approach. International Journal of Parallel, Emergent and Distributed Systems, 2009, 24, 311-330.	0.7	5
204	How GPUs can outperform ASICs for fast LDPC decoding. , 2009, , .		46
205	Applying the Stream-Based Computing Model to Design Hardware Accelerators: A Case Study. Lecture Notes in Computer Science, 2009, , 237-246.	1.0	11
206	Parallel LDPC Decoding on the Cell/B.E. Processor. Lecture Notes in Computer Science, 2009, , 389-403.	1.0	7
207	Heuristic Optimization Methods for Improving Performance of Recursive General Purpose Applications on GPUs. , 2008, , .		0
208	An RNS based Specific Processor for Computing the Minimum Sum-of-Absolute-Differences. , 2008, , .		14
209	Edge Stream Oriented LDPC Decoding. , 2008, , .		3
210	Application Specific Programmable IP Core for Motion Estimation: Technology Comparison Targeting Efficient Embedded Co-Processing Units. , 2008, , .		2
211	Distributed Web-based Platform for Computer Architecture Simulation. , 2008, , .		0
212	On-the-fly attestation of reconfigurable hardware. , 2008, , .		8
213	Efficient FPGA elliptic curve cryptographic processor over GF(2^m). , 2008, , .		3
214	Detection of 130nm magnetic particles by a portable electronic platform using spin valve and magnetic tunnel junction sensors. Journal of Applied Physics, 2008, 103, 07A310.	1.1	32
215	Design and implementation of a tool for modeling and programming deadlock free meta-pipeline applications. Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on, 2008, , .	1.0	0
216	A Parallel Algorithm for Advanced Video Motion Estimation on Multicore Architectures. , 2008, , .		12

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217	Massive parallel LDPC decoding on GPU. , 2008, , .		35
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