Chi-Ying Tsui

List of Publications by Year
in descending order

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175 papers	4,357 citations	147801 31 h-index	149698 56 g-index
177 all docs	177 docs citations	177 times ranked	3120 citing authors

#	Article	IF	Citations
1	Single-inductor multiple-output switching converters with time-multiplexing control in discontinuous conduction mode. IEEE Journal of Solid-State Circuits, 2003, 38, 89-100.	5.4	300
2	A pseudo-CCM/DCM SIMO switching converter with freewheel switching. IEEE Journal of Solid-State Circuits, 2003, 38, 1007-1014.	5.4	274
3	Analysis and Design Strategy of UHF Micro-Power CMOS Rectifiers for Micro-Sensor and RFID Applications. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 153-166.	0.1	270
4	A 13.56 MHz Wireless Power Transfer System With Reconfigurable Resonant Regulating Rectifier and Wireless Power Control for Implantable Medical Devices. IEEE Journal of Solid-State Circuits, 2015, 50, 978-989.	5.4	228
5	Integrated Low-Loss CMOS Active Rectifier for Wirelessly Powered Devices. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 1378-1382.	2.2	203
6	A VLSI architecture of a K-best lattice decoding algorithm for MIMO channels. , 0, , .		171
7	Low-power VLSI design for motion estimation using adaptive pixel truncation. IEEE Transactions on Circuits and Systems for Video Technology, 2000, 10, 669-678.	8.3	114
8	The Design of a Micro Power Management System for Applications Using Photovoltaic Cells With the Maximum Output Power Control. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1138-1142.	3.1	110
9	Ultra Fast Fixed-Frequency Hysteretic Buck Converter With Maximum Charging Current Control and Adaptive Delay Compensation for DVS Applications. IEEE Journal of Solid-State Circuits, 2008, 43, 815-822.	5.4	104
10	Power estimation methods for sequential logic circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 1995, 3, 404-416.	3.1	100
11	Vibration Energy Scavenging System With Maximum Power Tracking for Micropower Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 2109-2119.	3.1	90
12	Ultra-Low-Power Smart Electronic Nose System Based on Three-Dimensional Tin Oxide Nanotube Arrays. ACS Nano, 2018, 12, 6079-6088.	14.6	88
13	A system-on-chip EPC Gen-2 passive UHF RFID tag with embedded temperature sensor. , 2010, , .		78
14	A Novel Single-Inductor Dual-Input Dual-Output DCâ€“DC Converter With PWM Control for Solar Energy Harvesting System. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1693-1704.	3.1	77
15	An Integrated One-Cycle Control Buck Converter With Adaptive Output and Dual Loops for Output Error Correction. IEEE Journal of Solid-State Circuits, 2004, 39, 140-149.	5.4	75
16	Joint Routing and Sleep Scheduling for Lifetime Maximization of Wireless Sensor Networks. IEEE Transactions on Wireless Communications, 2010, 9, 2258-2267.	9.2	74
17	A System-on-Chip EPC Gen-2 Passive UHF RFID Tag With Embedded Temperature Sensor. IEEE Journal of Solid-State Circuits, 2010, , .	5.4	72
18	A 6.78-MHz Single-Stage Wireless Power Receiver Using a 3-Mode Reconfigurable Resonant Regulating Rectifier. IEEE Journal of Solid-State Circuits, 2017, 52, 1412-1423.	5.4	65

#	Article	IF	Citations
19	High-Throughput and Energy-Efficient Belief Propagation Polar Code Decoder. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1098-1111.	3.1	60
20	Gate-level power estimation using tagged probabilistic simulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1998, 17, 1099-1107.	2.7	58
21	Design of Sub-Gigahertz Reconfigurable RF Energy Harvester From â^'22 to 4 dBm With 99.8% Peak MPPT Power Efficiency. IEEE Journal of Solid-State Circuits, 2019, 54, 2601-2613.	5.4	55
22	A Single-Chip UHF RFID Reader in 0.18 $mu{hbox {m}}$ CMOS Process. IEEE Journal of Solid-State Circuits, 2008, 43, 1741-1754.	5.4	52
23	An Efficient Partial-Sum Network Architecture for Semi-Parallel Polar Codes Decoder Implementation. IEEE Transactions on Signal Processing, 2014, 62, 3165-3179.	5.3	52
24	Power efficient technology decomposition and mapping under an extended power consumption model. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1994, 13, 1110-1122.	2.7	44
25	Low-power state assignment targeting two- and multilevel logic implementations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1998, 17, 1281-1291.	2.7	42
26	A <emphasis emphasistype="smcaps">mux</emphasis>-based High-Performance Single-Cycle CMOS Comparator. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 591-595.	2.2	42
27	A Low-Latency List Successive-Cancellation Decoding Implementation for Polar Codes. IEEE Journal on Selected Areas in Communications, 2016, 34, 303-317.	14.0	41
28	A low complexity architecture of the V-BLAST system. , 0, , .		39
29	A Support Vector Regression (SVR)-Based Latency Model for Network-on-Chip (NoC) Architectures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 471-484.	2.7	38
30	Regulated Switched-Capacitor Doubler With Interleaving Control for Continuous Output Regulation. IEEE Journal of Solid-State Circuits, 2009, 44, 1112-1120.	5.4	35
31	A micro power management system and maximum output power control for solar energy harvesting applications. , 2007, , .		34
32	A Fully Integrated Analog Front End for Biopotential Signal Sensing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3800-3809.	5.4	34
33	Electrical stimulation at nanoscale topography boosts neural stem cell neurogenesis through the enhancement of autophagy signaling. Biomaterials, 2021, 268, 120585.	11.4	34
34	A programmable integrated digital controller for switching converters with dual-band switching and complex pole-zero compensation. IEEE Journal of Solid-State Circuits, 2005, 40, 772-780.	5.4	32
35	Wireless Power Transfer System With $SigmaDelta$- Modulated Transmission Power and Fast Load Response for Implantable Medical Devices. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 279-283.	3.0	32
36	A traffic-aware adaptive routing algorithm on a highly reconfigurable network-on-chip architecture. , 2012, , .		31

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37	An Inductor-less Micro Solar Power Management System Design for Energy Harvesting Applications. , 2007, , .		29
38	12.8 Wireless power transfer system using primary equalizer for coupling- and load-range extension in bio-implant applications. , 2015, , .		29
39	Dual Transduction Surface Acoustic Wave Gas Sensor for VOC Discrimination. IEEE Electron Device Letters, 2018, 39, 1920-1923.	3.9	28
40	An Energy Efficient Layered Decoding Architecture for LDPC Decoder. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1185-1195.	3.1	27
41	Power Management Analysis of Inductively-Powered Implants with 1X/2X Reconfigurable Rectifier. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 617-624.	5.4	27
42	Low-latency list decoding of polar codes with double thresholding. , 2015, , .		26
43	Reconfigurable Resonant Regulating Rectifier With Primary Equalization for Extended Coupling- and Loading-Range in Bio-Implant Wireless Power Transfer. IEEE Transactions on Biomedical Circuits and Systems, 2016, 9, 1-1.	4.0	26
44	A robust, input voltage adaptive and low energy consumption level converter for sub-threshold logic. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2007, , .	0.0	24
45	A 13.56MHz fully integrated 1X/2X active rectifier with compensated bias current for inductively powered devices. , 2013, , .		24
46	A High-Throughput Architecture of List Successive Cancellation Polar Codes Decoder With Large List Size. IEEE Transactions on Signal Processing, 2018, 66, 3859-3874.	5.3	24
47	An efficient Network-on-Chip (NoC) based multicore platform for hierarchical parallel genetic algorithms. , 2014, , .		23
48	A comprehensive and accurate latency model for Network-on-Chip performance analysis. , 2014, , .		23
49	Gate Control Strategies for High Efficiency Charge Pumps. , 0, , .		22
50	SparseNN: An energy-efficient neural network accelerator exploiting input and output sparsity. , 2018, , .		22
51	Low-Power Limited-Search Parallel State Viterbi Decoder Implementation Based on Scarce State Transition. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 1172-1176.	3.1	20
52	Design and analysis of on-chip charge pumps for micro-power energy harvesting applications. , 2011, , .		20
53	A â˜’12.3 dBm UHF Passive RFID Sense Tag for Grid Thermal Monitoring. IEEE Transactions on Industrial Electronics, 2019, 66, 8811-8820.	7.9	20
54	Vibration energy scavenging and management for ultra low power applications. , 2007, , .		19

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55	A 1.8 V single-inductor dual-output switching converter for power reduction techniques. , 0, , .		17
56	A WLAN 2.4-GHz RF energy harvesting system with reconfigurable rectifier for wireless sensor network. , 2016, , .		17
57	Integrated single-inductor dual-input dual-output boost converter for energy harvesting applications. , 2008, , .		16
58	Energy Harvesting and Power Delivery for Implantable Medical Devices. Foundations and Trends in Electronic Design Automation, 2013, 7, 179-246.	1.0	16
59	Low complexity belief propagation polar code decoder. , 2015, , .		16
60	Performance Evaluation of NoC-Based Multicore Systems. ACM Transactions on Design Automation of Electronic Systems, 2016, 21, 1-38.	2.6	16
61	Hardware decoders for polar codes: An overview. , 2016, , .		16
62	Optimal link scheduling on improving best-effort and guaranteed services performance in network-on-chip systems. , 2006, , .		15
63	Single-inductor multiple-output switching converters with bipolar outputs. , 0, , .		14
64	Disease Diagnosis-on-a-Chip. , 2014, , .		14
65	Concatenated LDPC-polar codes decoding through belief propagation. , 2017, , .		14
66	A Batteryless Vibration-based Energy Harvesting System for Ultra Low Power Ubiquitous Applications. , 2007, , .		13
67	Threshold Voltage Start-up Boost Converter for Sub-mA Applications. , 2008, , .		13
68	A single inductor dual input dual output DC-DC converter with hybrid supplies for solar energy harvesting applications. , 2009, , .		12
69	An adaptive wireless powering and data telemetry system for optic nerve stimulation. , 2014, , .		12
70	Low-latency approximate matrix inversion for high-throughput linear pre-coders in massive MIMO. , 2016, , .		12
71	A 10.6 pJÂ·K² Resolution FoM Temperature Sensor Using Astable Multivibrator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 869-873.	3.0	12
72	Analysis and Design Strategy of On-Chip Charge Pumps for Micro-power Energy Harvesting Applications. International Federation for Information Processing, 2012, , 158-186.	0.4	12

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73	Exploiting Dynamic Workload Variation in Low Energy Preemptive Task Scheduling. , 0, , .		11
74	Charge Redistribution Loss Consideration in Optimal Charge Pump Design. , 0, , .		11
75	A thermal-aware application specific routing algorithm for Network-on-Chip design. , 2011, , .		11
76	A high-throughput and energy-efficient RRAM-based convolutional neural network using data encoding and dynamic quantization. , 2018, , .		11
77	Analysis and Design of a Ripple Reduction Chopper Bandpass Amplifier. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1185-1195.	5.4	11
78	Improving the efficiency of power simulators by input vector compaction. , 0, , .		10
79	Adaptive tracking of optimal bit and power allocation for OFDM systems in time-varying channels. , 0, , .		10
80	Stable round-robin scheduling algorithms for high-performance input queued switches. , 0, , .		10
81	Ultra-low voltage power management and computation methodology for energy harvesting applications. , 0, , .		10
82	High Efficiency Cross-Coupled Doubler with No Reversion Loss. , 0, , .		10
83	A single inductor DIDO DC-DC converter for solar energy harvesting applications using band-band control. , 2010, , .		10
84	FSNoC: A Flit-Level Speedup Scheme for Network on-Chips Using Self-Reconfigurable Bidirectional Channels. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1854-1867.	3.1	10
85	An implementation of list successive cancellation decoder with large list size for polar codes. , 2017, , .		10
86	UHF energy harvesting system using reconfigurable rectifier for wireless sensor network. , 2015, , .		9
87	Low-Complexity List Successive-Cancellation Decoding of Polar Codes Using List Pruning. , 2016, , .		9
88	A threshold-based algorithm and VLSI architecture of a K-best Lattice Decoder for MIMO Systems. , 0, , .		8
89	An energy-adaptive MPPT power management unit for micro-power vibration energy harvesting. , 2008, , .		8
90	Solar energy harvesting system design using re-configurable charge pump. , 2012, , .		8

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91	Efficient wireless power transmission technology based on above-CMOS integrated (ACI) high quality inductors. , 2014, , .		8
92	21.7 A 6.78MHz 6W wireless power receiver with a 3-level 1Ã— / Â½ Ã— / 0Ã— reconfigurable resonant regulating rectifier. , 2016, , .		8
93	Efficient Partial-Sum Network Architectures for List Successive-Cancellation Decoding of Polar Codes. IEEE Transactions on Signal Processing, 2018, 66, 3848-3858.	5.3	8
94	A Low-Power Compression-Based CMOS Image Sensor With Microshift-Guided SAR ADC. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1350-1354.	3.0	8
95	Tight Compression: Compressing CNN Model Tightly Through Unstructured Pruning and Simulated Annealing Based Permutation. , 2020, , .		8
96	Reducing power consumption of turbo-code decoder using adaptive iteration with variable supply voltage. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2001, 9, 34-41.	3.1	7
97	A Scalable Frame-Level Pipelined Architecture for FSBM Motion Estimation. , 2007, , .		7
98	Low-Complexity Rotated QAM Demapper for the Iterative Receiver Targeting DVB-T2 Standard. , 2012, , .		7
99	Optic Nerve Stimulation System with Adaptive Wireless Powering and Data Telemetry. Micromachines, 2017, 8, 368.	2.9	7
100	Minimizing the dynamic and sub-threshold leakage power consumption using least leakage vector-assisted technology mapping. The Integration VLSI Journal, 2008, 41, 76-86.	2.1	6
101	A Low Energy Two-Step Successive Approximation Algorithm for ADC Design. , 2008, , .		6
102	A low energy two-step successive approximation algorithm for ADC design. , 2009, , .		6
103	An indoor solar energy harvesting system using dual mode SIDO converter with fully digital time-based MPPT. , 2016, , .		6
104	BiLink: A high performance NoC router architecture using bi-directional link with double data rate. The Integration VLSI Journal, 2016, 55, 30-42.	2.1	6
105	A low-offset dynamic comparator with area-efficient and low-power offset cancellation. , 2017, , .		6
106	Energy-Efficient Dual-Node-Upset-Recoverable 12T SRAM for Low-Power Aerospace Applications. IEEE Access, 2023, 11, 20184-20195.	4.2	6
107	Minimizing energy consumption of multiple-processors-core systems with simultaneous task allocation, scheduling and voltage assignment. , 0, , .		5
108	A low power layered decoding architecture for LDPC decoder implementation for IEEE 802.11n LDPC codes. , 2008, , .		5

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109	BHNN: A memory-efficient accelerator for compressing deep neural networks with blocked hashing techniques. , 2017, , .		5
110	Energy-Aware Synthesis of Networks-on-Chip Implemented with Voltage Islands. Proceedings - Design Automation Conference, 2007, , .	0.0	5
111	An efficient and reconfigurable VLSI architecture for different block matching motion estimation algorithms. , 0, , .		4
112	Towards the capability of providing power-area-delay trade-off at the register transfer level. , 0, , .		4
113	Finite state machine partitioning for low power. , 0, , .		4
114	Low power ACS unit design for the Viterbi decoder [CDMA wireless systems]. , 0, , .		4
115	Re-configurable bus encoding scheme for reducing power consumption of the cross coupling capacitance for deep sub-micron instruction bus. , 0, , .		4
116	A low power Viterbi decoder implementation using scarce state transition and path pruning scheme for high throughput wireless applications. , 2006, , .		4
117	An Ultra Fast Fixed Frequency Buck Converter with Maximum Charging Current Control and Adaptive Delay Compensation for DVS Applications. , 2007, , .		4
118	Improving the hardware utilization efficiency of partially parallel LDPC decoder with scheduling and sub-matrix decomposition. , 2009, , .		4
119	A low-complexity image compression algorithm for Address-Event Representation (AER) PWM image sensors. , 2011, , .		4
120	A novel offset cancellation technique for dynamic comparator latch. , 2012, , .		4
121	Polyimide-Based Flexible 3-Coil Inductive Link Design and Optimization. , 2018, , .		4
122	Low Power Rake Receiver and Viterbi Decoder Design for CDMA Applications. Wireless Personal Communications, 2000, 14, 49-64.	2.7	3
123	VLSI implementation of rake receiver for IS-95 CDMA testbed using FPGA. , 0, , .		3
124	Optimal link scheduling on improving best-effort and guaranteed services performance in network-on-chip systems. Proceedings - Design Automation Conference, 2006, , .	0.0	3
125	Corrections to “Analysis and Design Strategy of UHF Micro-Power CMOS Rectifiers for Micro-Sensor and RFID Applications”. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 1406-1406.	0.1	3
126	An inductor-less MPPT design for light energy harvesting systems. , 2009, , .		3

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127	A hybrid algorithm and its re-configurable architecture for MIMO detector. , 2009, , .		3
128	Maximizing the harvested energy for micro-power applications through efficient MPPT and PMU design. , 2010, , .		3
129	A 13.56MHz wireless power transfer system with reconfigurable resonant regulating rectifier and wireless power control for implantable medical devices. , 2014, , .		3
130	A low-power chopper bandpass amplifier for biopotential sensors. , 2016, , .		3
131	LRADNN: High-throughput and energy-efficient Deep Neural Network accelerator using Low Rank Approximation. , 2016, , .		3
132	Tight Compression: Compressing CNN Through Fine-Grained Pruning and Weight Permutation for Efficient Implementation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 644-657.	2.7	3
133	VLSI design of an ATM switch with automatic fault detection. , 0, , .		2
134	A gate duplication technique for timing optimization. Canadian Journal of Electrical and Computer Engineering, 2003, 28, 37-40.	2.0	2
135	Dynamic reconfigurable bus encoding scheme for reducing the energy consumption of deep sub-micron instruction bus. , 0, , .		2
136	A charge based computation system and control strategy for energy harvesting applications. , 0, , .		2
137	A Mixed-Signal Architecture of Channel Select Filtering with Oversampled ADC for Multi-Standard RFID Reader Receiver. , 2007, , .		2
138	System level power optimizations for EPC RFID tags to improve sensitivity using load power shaping and operation scheduling. , 2010, , .		2
139	Analysis of the heat removal capability of the power distribution network in 3D ICs. , 2010, , .		2
140	A fast variable block size motion estimation algorithm with refined search range for a two-layer data reuse scheme. , 2015, , .		2
141	An Implantable Medical Device for Transcorneal Electrical Stimulation: Packaging Structure, Process Flow, and Toxicology Test. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2016, , 1-7.	2.5	2
142	On Path Memory in List Successive Cancellation Decoder of Polar Codes. , 2018, , .		2
143	Room-Temperature Dual-mode CMOS Gas-FET Sensor for Diabetes Detection. , 2018, , .		2
144	A single-inductor dual-output integrated DC/DC boost converter for variable voltage scheduling. , 0, , .		1

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145	A pseudo-CCM/DCM SIMO switching converter with freewheel switching. , 0, , .		1
146	Performance study of OFDM receiver using FFT based on log number system. , 0, , .		1
147	Simultaneous task allocation, scheduling and voltage assignment for multiple-processors-core systems using mixed integer nonlinear programming. , 0, , .		1
148	Low Complexity SST Viterbi Decoder. , 2006, , .		1
149	Low energy level converter design for sub-V<inf>th</inf> logics. , 2009, , .		1
150	Efficient iterative receiver for LDPC coded wireless IPTV system. , 2011, , .		1
151	Thermal modeling of three-dimensional integrated circuits considering the thermal removal capability of different TSVs. , 2011, , .		1
152	A flit-level speedup scheme for network-on-chips using self-reconfigurable bi-directional channels. , 2012, , .		1
153	A new charge pump analysis and efficiency optimization method for on-chip charge pump. , 2012, , .		1
154	Low-latency MAP demapper architecture for coded modulation with iterative decoding. , 2014, , .		1
155	Fluxless packaging of an implantable medical device for transcorneal electrical stimulation. , 2015, , .		1
156	A Two-Staged Adaptive Successive Cancellation List Decoding for Polar Codes. , 2019, , .		1
157	Low power motion estimation design using adaptive pixel truncation. , 0, , .		0
158	Composite interference cancellation scheme for CDMA systems. , 0, , .		0
159	Low power controller optimization based on data path pattern extraction. , 0, , .		0
160	Low power 2-D array VLSI architecture for block matching motion estimation using computation suspension. , 0, , .		0
161	VLSI implementation of a switch fabric for mixed ATM and IP traffic. , 0, , .		0
162	A pseudo-CCM/DCM SIMO switching converter with freewheel switching. , 0, , .		0

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163	Bi-directional integrated charge pumps. , 0, , .		0
164	Minimizing energy consumption of hard real-time systems with simultaneous tasks scheduling and voltage assignment using statistical data. , 2004, , .		0
165	Least leakage vector assisted technology mapping for total power optimization. , 0, , .		0
166	A data discarding framework for reducing the energy consumption of Viterbi decoder in decoding broadcasted wireless multi-resolution JPEG2000 images. , 2005, , .		0
167	Ultra-low voltage power management circuit and computation methodology for energy harvesting applications. , 0, , .		0
168	An SC voltage regulator with novel area-efficient continuous output regulation by dual-branch interleaving control scheme. , 2008, , .		0
169	A fault-tolerant NoC using combined link sharing and partial fault link utilization scheme. , 2011, , .		0
170	Low energy multi-stage level converter for sub-threshold logic. IET Computers and Digital Techniques, 2011, 5, 375.	1.2	0
171	A fault-tolerant network-on-chip design using dynamic reconfiguration of partial-faulty routing resources. , 2011, , .		0
172	Rate and Power Allocation for 2-Level Superposition Coded Modulation Supporting Both Unicast and Multicast Traffic. , 2012, , .		0
173	Performance evaluation of multicore systems: From traffic analysis to latency predictions (Embedded) Tj ETQq1 1 0.784314 rgBT /Ove		0
174	A fast intermode decision algorithm based on analysis of inter prediction residual. , 2014, , .		0
175	A Simplified PWM Controller for Wireless Power Receiver Using a 3-Mode Reconfigurable Resonant Regulating Rectifier. , 2018, , .		0