Jose Silva-Martinez

List of Publications by Year
in descending order

55 papers	1,365 citations	516710 16 h-index	345221 36 g-index
55 all docs	55 docs citations	55 times ranked	948 citing authors

#	Article	IF	Citations
1	An Interference-Tolerant Synchronization Scheme for Wireless Communication Systems Based on Direct Sequence Spread Spectrum. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 415-427.	5.4	2
2	Recent Advances on Linear Low-Dropout Regulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 568-573.	3.0	13
3	An Ultrafast Multibit/Stage Pipelined ADC Testing and Calibration Method. IEEE Transactions on Instrumentation and Measurement, 2020, 69, 729-738.	4.7	4
4	A 12-Bit 125-MS/s 2.5-Bit/Cycle SAR-Based Pipeline ADC Employing a Self-Biased Gain Boosting Amplifier. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3618-3629.	5.4	5
5	An Efficient Sinusoid-Like Pseudo Random Sequence Modulator/Demodulator System With Reduced Adjacent Channel Leakage and High Rejection to Random and Systematic Interference. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3790-3803.	5.4	1
6	A 245-mA Digitally Assisted Dual-Loop Low-Dropout Regulator. IEEE Journal of Solid-State Circuits, 2020, 55, 2140-2150.	5.4	18
7	A 13-Bit 260MS/s Power-Efficient Pipeline ADC Using a Current-Reuse Technique and Interstage Gain and Nonlinearity Errors Calibration. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3373-3383.	5.4	11
8	A 27.7 fJ/conv-step 500 MS/s 12-Bit Pipelined ADC Employing a Sub-ADC Forecasting Technique and Low-Power Class AB Slew Boosted Amplifiers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3352-3364.	5.4	13
9	A 3â€“6-GHz Highly Linear I-Channel Receiver With Over +3.0-dBm In-Band P_{1dB} and 200-MHz Baseband Bandwidth Suitable for 5G Wireless and Cognitive Radio Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3134-3147.	5.4	16
10	A 128-Tap Highly Tunable CMOS IF Finite Impulse Response Filter for Pulsed Radar Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1192-1203.	3.1	3
11	A Continuous-Time MASH 1-1-1 Deltaâ€“Sigma Modulator With FIR DAC and Encoder-Embedded Loop-Unrolling Quantizer in 40-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 756-767.	3.1	15
12	Practical Design Considerations for Broadband Cognitive Radio Systems: Co-existence. , 2018, , .		1
13	Practical Considerations for Broadband Cognitive Radio Systems: On-chip Spectrum Sensing. , 2018, , .		0
14	Operational Transconductance Amplifier With Class-B Slew-Rate Boosting for Fast High-Performance Switched-Capacitor Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3769-3779.	5.4	23
15	A 44-fJ/Conversion Step 200-MS/s Pipeline ADC Employing Current-Mode MDACs. IEEE Journal of Solid-State Circuits, 2018, 53, 3280-3292.	5.4	14
16	A Low-Power Digitizer for Back-Illuminated 3-D-Stacked CMOS Image Sensor Readout With Passing Window and Double Auto-Zeroing Techniques. IEEE Journal of Solid-State Circuits, 2017, 52, 1591-1604.	5.4	25
17	Compressed Level Crossing Sampling for Ultra-Low Power IoT Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2495-2507.	5.4	9
18	Blocker-Tolerant and High-Sensitivity $Delta Sigma $ Correlation Digitizer for Radar and Coherent Receiver Applications. IEEE Transactions on Microwave Theory and Techniques, 2017, 65, 3453-3463.	4.6	2

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19	A 75-MHz Continuous-Time Sigmaâ€“Delta Modulator Employing a Broadband Low-Power Highly Efficient Common-Gate Summing Stage. IEEE Journal of Solid-State Circuits, 2017, 52, 657-668.	5.4	22
20	A Wideband Low-Power-Consumption 22â€“32.5-GHz 0.18- $mu ext{m}$ BiCMOS Active Balun-LNA With IM2 Cancellation Using a Transformer-Coupled Cascode-Cascade Topology. IEEE Transactions on Microwave Theory and Techniques, 2017, 65, 536-547.	4.6	19
21	A 43-mW MASH 2-2 CT $Sigma Delta$ Modulator Attaining 74.4/75.8/76.8 dB of SNDR/SNR/DR and 50 MHz of BW in 40-nm CMOS. IEEE Journal of Solid-State Circuits, 2017, 52, 448-459.	5.4	36
22	A 200MSPS time-interleaved 12-bit ADC system with digital calibration. , 2017, , .		1
23	Algorithmic-pipelined ADC with a modified residue curve for better linearity. , 2017, , .		7
24	A digital-circuit-based evolutionary-computation algorithm for time-interleaved ADC background calibration. , 2016, , .		11
25	A 4 Bit Continuous-Time <inline-formula> <tex-math notation="LaTeX">$Sigma Delta $ </tex-math> </inline-formula> Modulator With Fully Digital Quantization Noise Reduction Algorithm Employing a 7 Bit Quantizer. IEEE Journal of Solid-State Circuits, 2016, 51, 1398-1409.	5.4	14
26	A 0.6ps jitter 2–16 GHz 130nm CMOS frequency synthesizer for broadband applications. , 2015, , .		0
27	A Process-Variation Resilient Current Mode Logic With Simultaneous Regulations for Time Constant, Voltage Swing, Level Shifting, and DC Gain Using Time-Reference-Based Adaptive Biasing Chain. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 198-202.	3.1	1
28	A 44.9% PAE digitally-assisted linear power amplifier in 40 nm CMOS. , 2014, , .		2
29	Blocker tolerant wideband continuous time sigma-delta modulator for wireless applications. , 2014, , .		0
30	Design techniques for external capacitor-less LDOs with high PSR over wide frequency range. , 2014, , .		5
31	External Capacitor-Less Low Drop-Out Regulator With 25 dB Superior Power Supply Rejection in the 0.4â€“4 MHz Range. IEEE Journal of Solid-State Circuits, 2014, 49, 486-501.	5.4	150
32	A current-mode flash ADC for low-power continuous-time sigma delta modulators. , 2013, , .		4
33	Dual-Level Adaptive Supply Voltage System for Variation Resilience. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1041-1052.	3.1	4
34	Efficient calibration scheme for high-resolution pipelined ADCs. , 2013, , .		1
35	An external capacitor-less low drop-out regulator with superior PSR and fast transient response. , 2013, , .		8
36	An LC Quadrature VCO Using Capacitive Source Degeneration Coupling to Eliminate Bi-Modal Oscillation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1871-1879.	5.4	22

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37	Blocker and jitter tolerant wideband ΣΔ modulators. , 2012, , .		0
38	Mismatch reduction technique for transistors with minimum channel length. Analog Integrated Circuits and Signal Processing, 2012, 70, 429-435.	1.4	4
39	Inductorless wideband CMOS LNAs with nonlinearity cancellation. , 2011, , .		3
40	A large-signal blocker robust transimpedance amplifier for coexisting radio receivers in 45nm CMOS. , 2011, , .		5
41	Electrothermal Design Procedure to Observe RF Circuit Power and Linearity Characteristics With a Homodyne Differential Temperature Sensor. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 458-469.	5.4	30
42	A 25 MHz Bandwidth 5th-Order Continuous-Time Low-Pass Sigma-Delta Modulator With 67.7 dB SNDR Using Time-Domain Quantization and Feedback. IEEE Journal of Solid-State Circuits, 2010, 45, 1795-1808.	5.4	48
43	An On-Chip Loopback Block for RF Transceiver Built-In Test. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 444-448.	3.0	14
44	A 1.8V, sub-mW, over 100% locking range, divide-by-3 and 7 complementary-injection-locked 4 GHz frequency divider. , 2009, , .		11
45	A Broadband CMOS Amplitude Detector for On-Chip RF Measurements. IEEE Transactions on Instrumentation and Measurement, 2008, 57, 1470-1477.	4.7	95
46	A CMOS differential noise cancelling low noise transconductance amplifier. , 2008, , .		8
47	Applications of Multipath Transform-Domain Charge-Sampling Wide-Band Receivers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 309-313.	3.0	17
48	A low power 1.3GHz dual-path current mode Gm-C filter. , 2008, , .		1
49	Steady-State Analysis of Phase-Locked Loops Using Binary Phase Detector. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 474-478.	2.2	10
50	Full On-Chip CMOS Low-Dropout Voltage Regulator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2007, 54, 1879-1890.	5.4	420
51	A 63 dB SNR, 75-mW Bandpass RF $SigmaDelta$ ADC at 950 MHz Using 3.8-GHz Clock in 0.25-$mu{hbox {m}}$ SiGe BiCMOS Technology. IEEE Journal of Solid-State Circuits, 2007, 42, 269-279.	5.4	58
52	A Fully Differential Low-Power Divide-by-8 Injection-Locked Frequency Divider Up to 18 GHz. IEEE Journal of Solid-State Circuits, 2007, 42, 583-591.	5.4	46
53	Estimation of Aliasing Effects Due to Periodical Nonuniform Individual Sampling in High-<emphasis>Q</emphasis> Switched-Capacitor Filters. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 387-391.	2.2	1
54	A Highly Linear Low-Noise Amplifier. IEEE Transactions on Microwave Theory and Techniques, 2006, 54, 4079-4085.	4.6	91

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55	Quasi Rail-to-Rail Very Low-Voltage OPAMP With a Single pMOS Input Differential Pair. IEEE Transactions on Circuits and Systems II: Express Briefs, 2006, 53, 1175-1179.	3.0	21