Jianhui Wu

List of Publications by Year
in descending order

103	413	840119 11	996533 15
papers	citations	h-index	g-index

103	103	103	333
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A 400-Î¼W IoT Low-IF Voltage-Mode Receiver Front-End With Charge-Sharing Complex Filter. IEEE Journal of Solid-State Circuits, 2022, 57, 1957-1967.	3.5	1
2	Correlation-Based Background Calibration of Bit Weight in SAR ADCs Using DAS Algorithm. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1063-1067.	2.2	6
3	A Background Correlation-Based Timing Skew Estimation Method for Time-Interleaved ADCs. IEEE Access, 2021, 9, 45730-45739.	2.6	12
4	Background Calibration of Capacitor Mismatch and Gain Error in Pipelined-SAR ADC Using Partially Split Structure. , 2021, , .		2
5	A Low-Energy and Area-Efficient Vaq-Based Switching Scheme with Capacitor-Splitting Structure for SAR ADCs. Circuits, Systems, and Signal Processing, 2021, 40, 4106-4126.	1.2	6
6	Two-Stage Difference-Based Estimation Method for Timing Skew in TI-ADCs. , 2021, , .		0
7	A 4.8-dB NF, 440-Î¼W Bluetooth Receiver Front-End With a Cascode Noise Canceling LNTA. IEEE Microwave and Wireless Components Letters, 2021, 31, 489-492.	2.0	4
8	New Failure Mechanism Induced by Current Limit for Superjunction MOSFET Under Single-Pulse UIS Stress. IEEE Transactions on Electron Devices, 2021, 68, 3483-3489.	1.6	5
9	An energy-efficient switching scheme based on the improved semi-resting DAC structure and floating-capacitor technique for SAR ADC. Analog Integrated Circuits and Signal Processing, 2021, 108, 679-687.	0.9	3
10	Energy-efficient switching scheme for SAR ADCs using two reference levels. Analog Integrated Circuits and Signal Processing, 2021, 106, 661-667.	0.9	2
11	A 400-ÂµW Low-IF IoT Receiver Front-End with Tunable Charge-Sharing Complex Filter. , 2021, , .		1
12	A Low Phase Noise Open Loop Fractional-N Frequency Synthesizer With Injection Locking Digital Phase Modulator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 455-459.	2.2	2
13	A Review on Calibration Methods of Timing-Skew in Time-Interleaved ADCs. Journal of Circuits, Systems and Computers, 2020, 29, 2030002.	1.0	9
14	Energy efficient switching scheme based on MSB-split structure for SAR ADC. Analog Integrated Circuits and Signal Processing, 2020, 105, 135-139.	0.9	2
15	Complete Avalanche Process and Failure Mechanism of Trench-Gate FS-IGBT Under Unclamped Inductive Switching by Using Infrared Visualization Method. IEEE Transactions on Electron Devices, 2020, 67, 3908-3911.	1.6	9
16	Low Voltage Delay Element with Dynamic Biasing Technique for Fully Integrated Cold-Start in Battery-Assistance DC Energy Harvesting Systems. Applied Sciences (Switzerland), 2020, 10, 6993.	1.3	2
17	A 99.82% energy-saving and 87.5% area-reducing Vaq-based switching scheme with capacitor-splitting structure for SAR ADC. Analog Integrated Circuits and Signal Processing, 2020, 105, 297-303.	0.9	1
18	Mismatch Insensitive Voltage Level Shifter Based on Two Feedback Loops. Electronics (Switzerland), 2020, 9, 1391.	1.8	1

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19	An energy-efficient switching scheme with low common-mode voltage variation and no-capacitor-splitting DAC for SAR ADC. Analog Integrated Circuits and Signal Processing, 2020, 104, 93-101.	0.9	5
20	Digital background calibration technique for pipelined SAR ADCs with detectâ€andâ€switching algorithm. Electronics Letters, 2020, 56, 533-536.	0.5	0
21	Background calibration based on signalâ€dependent dithering for pipelined SAR ADCs exploiting noise quantiser technique. Electronics Letters, 2020, 56, 227-229.	0.5	3
22	A 99.79% energy saving switching scheme without third reference level and reset energy for SAR ADC. Analog Integrated Circuits and Signal Processing, 2020, 102, 667-673.	0.9	1
23	Background Calibration of Bit Weights in Pipelined-SAR ADCs Using Paired Comparators. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1074-1078.	2.1	14
24	A Low-Spur MASH Delta-Sigma Modulator With an Adaptive Length Extension Technique. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2818-2822.	2.2	0
25	Modeling of High-Resolution Data Converter: Two-Step Pipelined-SAR ADC based on ISDM. Electronics (Switzerland), 2020, 9, 137.	1.8	4
26	Breakdown Voltage Walk-in Phenomenon and Optimization for the Trench-Gate p-Type VDMOS Under Single Avalanche Stress. IEEE Transactions on Electron Devices, 2020, 67, 2445-2450.	1.6	4
27	Low Voltage Cold Start-Up Ring Oscillator with Dynamic Body Biasing Technique for Battery-Assistance DC Energy Harvesting Systems. , 2020, , .		0
28	A Low-Power 0.6-V Quadrature VCO With a Coupling Current Reuse Technique. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 202-206.	2.2	11
29	A 12-bit 350 MS/s Single-Channel Pipeline ADC with 75 dB SFDR in 0.18 Î¼m BiCMOS. Journal of Circuits, Systems and Computers, 2019, 28, 1950044.	1.0	1
30	A Review of CMOS Variable Gain Amplifiers and Programmable Gain Amplifiers. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2019, 36, 484-500.	2.1	6
31	A digital-mixing-based method for timing skew estimation in time-interleaved ADCs. Microelectronics Journal, 2019, 91, 46-52.	1.1	4
32	Ditherâ€based background calibration of capacitor mismatch and gain error in pipelined noise shaping successive approximation register ADCs. Electronics Letters, 2019, 55, 984-986.	0.5	8
33	A low energy switching scheme for SAR ADC with MSB-splitting DAC structure. Analog Integrated Circuits and Signal Processing, 2019, 100, 199-203.	0.9	5
34	Differenceâ€equalisation based estimation of timing skew for timeâ€interleaved ADCs in communication systems. Electronics Letters, 2019, 55, 1331-1333.	0.5	0
35	A 12-bit 250 MS/s pipeline ADC with 78 dB SFDR in 0.13-Âµm CMOS. International Journal of Electronics, 2018, 105, 1248-1260.	0.9	2
36	A Compact Low-Power Biquad for Active-<inline-formula> <tex-math notation="LaTeX">RC </tex-math> </inline-formula> Complex Filter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 709-713.	2.2	17

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37	Two-step Vcm-based MS switching method with dual-capacitive arrays for SAR ADCs. Analog Integrated Circuits and Signal Processing, 2018, 94, 155-160.	0.9	7
38	A Light CNN based Method for Hand Detection and Orientation Estimation. , 2018, , .		5
39	Analysis and design of highly linear Gmâ€“TIA PGA with flat gain response. Analog Integrated Circuits and Signal Processing, 2018, 97, 135-141.	0.9	0
40	A 370Î¼W Ring VCO Based Injection-Locked Frequency Synthesizer for GPS Receiver. , 2018, , .		1
41	A 2.4 GS/s Time Interleaved ADC with 76 dB SFDR in 0.18 Î¼m BiCMOS. , 2018, , .		0
42	A self-refereed design-for-test structure of CP-PLL for on-chip jitter measurement. IEICE Electronics Express, 2018, 15, 20171215-20171215.	0.3	0
43	A 12-bit 1.0/2.0ÂGS/s Pipeline ADC in 0.18ÂÂµm SiGe BiCMOS. International Journal of Electronics, 2018, 105, 2114-2127.	0.9	3
44	A 1.2-V Self-Reconfigurable Recursive Mixer With Improved IF Linearity in 130-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 36-40.	2.2	5
45	A 35-dBm OIP3 CMOS Constant Bandwidth PGA With Extended Input Range and Improved Common-Mode Rejection. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 922-926.	2.2	12
46	A Low Offset Dynamic Comparator with Offset Elimination Circuit. Journal of Circuits, Systems and Computers, 2017, 26, 1750115.	1.0	0
47	Energy-efficient switching scheme for ultra-low voltage SAR ADC. Analog Integrated Circuits and Signal Processing, 2017, 90, 507-511.	0.9	14
48	Digital background calibration of pipeline ADC based on correlation. International Journal of Electronics, 2017, , 1-12.	0.9	3
49	A self-calibrated multiphase timing system in time-interleaved ADC. , 2017, , .		2
50	A high speed pipeline ADC with 78-dB SFDR in 0.18 um BiCMOS. , 2016, , .		1
51	A CMOS low power fast-settling AGC amplifier based on integrated RSSI. Analog Integrated Circuits and Signal Processing, 2016, 87, 379-387.	0.9	3
52	Builtâ€in selfâ€test structure for fault detection of chargeâ€pump phaseâ€locked loop. IET Circuits, Devices and Systems, 2016, 10, 317-321.	0.9	4
53	Ditheringâ€based calibration of capacitor mismatch in SAR ADCs. Electronics Letters, 2016, 52, 1598-1600.	0.5	3
54	1.2 V CMOS temperature compensated logarithmic converter based on translinear circuit. Electronics Letters, 2016, 52, 1742-1744.	0.5	3

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55	0.6â€V 2.1â€mW RF receiver based on passive mixing and masterâ€“slave commonâ€mode rejection technique in 65Ânm CMOS. Electronics Letters, 2016, 52, 335-336.	0.5	7
56	A survey on aggregating methods for action recognition with dense trajectories. Multimedia Tools and Applications, 2016, 75, 5701-5717.	2.6	15
57	A highly linear programmable gain amplifier with level shifter and class AB output stage for bluetooth low energy. , 2015, , .		1
58	A 433ÂMHz â^'104ÂdBm OOK/ASK receiver with the dynamic range of 95ÂdB in 0.18-Âµm CMOS process. Analog Integrated Circuits and Signal Processing, 2015, 82, 189-196.	0.9	0
59	A 2.4-GHz All-Digital PLL With a 1-ps Resolution 0.9-mW Edge-Interchanging-Based Stochastic TDC. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 917-921.	2.2	13
60	A Review of LC-Based Digitally Controlled Oscillator with High Frequency Resolution. Journal of Circuits, Systems and Computers, 2015, 24, 1530002.	1.0	2
61	Digitalâ€domain dualâ€calibration for singleâ€ended successive approximation register ADCs. Electronics Letters, 2015, 51, 1161-1163.	0.5	3
62	CMOS temperature compensated logarithmic converter based on masterâ€“slave control. Electronics Letters, 2014, 50, 1574-1575.	0.5	3
63	A simplified feature line approach for face recognition. , 2014, , .		0
64	A high performance 2.4 GHz GaAs HBT class J power amplifier. , 2014, , .		2
65	The Influence of the Number of Relay Antennas on the Secure DoF with Active Cooperation. Frequenz, 2014, 68, .	0.6	0
66	An ADPLL with a MASH 1-1-1 ΔΣ Time-digital converter. , 2014, , .		0
67	A novel temperature compensating method of Logarithmic Amplifier in RSSI. , 2014, , .		1
68	A Low-Power 2.4-GHz Receiver Front End With a Lateral Current-Reusing Technique. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 564-568.	2.2	10
69	A Multiple-Stage Parallel Replica-Bitline Delay Addition Technique for Reducing Timing Variation of SRAM Sense Amplifiers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 264-268.	2.2	10
70	A low-cost built-in self-test for CP-PLL based on TDC. IEICE Electronics Express, 2014, 11, 20140247-20140247.	0.3	2
71	A low power dB-linear RSSI based on logarithmic amplifier. IEICE Electronics Express, 2014, 11, 20140431-20140431.	0.3	5
72	A tunable Gm-C polyphase filter with high linearity and automatic frequency calibration. IEICE Electronics Express, 2014, 11, 20140794-20140794.	0.3	6

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73	A methodology of fault detection using design for testability of CP-PLL. , 2014, , .		3
74	A high PSRR CMOS voltage reference with 1.2ÂV operation. Analog Integrated Circuits and Signal Processing, 2013, 77, 79-86.	0.9	6
75	Target Detection in Bistatic Radar Networks: Node Placement and Repeated Security Game. IEEE Transactions on Wireless Communications, 2013, 12, 1279-1289.	6.1	17
76	An all-digital Built-In Self-Test for Charge-Pump Phase-Locked Loops. , 2013, , .		4
77	A high-resolution stochastic time-to-digital converter with edge-interchange scheme. IEICE Electronics Express, 2013, 10, 20130211-20130211.	0.3	2
78	A 2.4GHz GaAs HBT stacked power amplifier with inductance compensation. IEICE Electronics Express, 2013, 10, 20130470-20130470.	0.3	0
79	A MASH 1-1-1 Î”Î£ time-to-digital converter based on two-stage time quantization. IEICE Electronics Express, 2013, 10, 20130729-20130729.	0.3	0
80	A low-power high-speed true single phase clock divide-by-2/3 prescaler. IEICE Electronics Express, 2013, 10, 20120913-20120913.	0.3	12
81	Secure Communication of the Multi-Antenna Channel Using Cooperative Relaying and Jamming. IEICE Transactions on Communications, 2013, E96.B, 948-955.	0.4	0
82	An optimized QFP structure for use in radio frequency multi-chip module applications. IEICE Electronics Express, 2012, 9, 1666-1674.	0.3	0
83	Improved timing carrier synchronizer and error controller for wireless multimedia sensor networks. , 2012, , .		0
84	A power reduction technique for multi-modulus divider. International Journal of Electronics, 2012, 99, 211-224.	0.9	1
85	SC-MAC: A sender-centric asynchronous MAC protocol for burst traffic in wireless sensor networks. , 2012, , .		3
86	A high-resolution DCO with MOS capacitors. , 2012, , .		2
87	All-Digital Wide Range Precharge Logic 50% Duty Cycle Corrector. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 760-764.	2.1	21
88	1ÂMHzâ€“3.5ÂGHz, wide range input duty 50% output duty cycle corrector. Analog Integrated Circuits and Signal Processing, 2012, 71, 531-538.	0.9	1
89	A 1.78â€“3.05ÂGHz fractional-N frequency synthesizer with power reduced multi-modulus divider. Analog Integrated Circuits and Signal Processing, 2012, 72, 97-109.	0.9	3
90	Digital Background Calibration Techniques for Pipelined ADC Based on Comparator Dithering. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 239-243.	2.2	26

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91	Wireless Secure Communications via Cooperative Relaying and Jamming. IEICE Transactions on Communications, 2012, E95.B, 2774-2784.	0.4	0
92	Multi-Antenna Secure Communications via Selective Diversity. IEICE Transactions on Communications, 2012, E95-B, 587-590.	0.4	0
93	Process-temperature-frequency adaptive voltage scaled SRAM system for power reduction. , 2011, , .		0
94	Modeling and design of coplanar structure in QFP80 package for RFIC applications. , 2011, , .		0
95	A CMOS voltage controlled oscillator topology for suppression of flicker noise up-conversion. IEICE Electronics Express, 2011, 8, 1056-1063.	0.3	0
96	Contributions to the analysis of deterministic noise on ADPLL jitter performance. Analog Integrated Circuits and Signal Processing, 2011, 67, 331-338.	0.9	1
97	Jitter and phase noise of ADPLL due to PSN with deterministic frequency. International Journal of Electronics, 2011, 98, 1259-1268.	0.9	0
98	Wide division ratio range programmable frequency divider with close-to-50% output duty-cycle. International Journal of Electronics, 2011, 98, 1239-1246.	0.9	0
99	A wide division-ratio range programmable frequency divider with driving-capability improved. Analog Integrated Circuits and Signal Processing, 2010, 63, 509-514.	0.9	3
100	An adaptive energy-efficient and low-latency MAC protocol for wireless sensor networks. Journal of Communications and Networks, 2010, 12, 510-517.	1.8	7
101	Improved CMOS continuous programmable divider. International Journal of Electronics, 2009, 96, 683-689.	0.9	1
102	Analysis of Jitter in CMOS Ring Oscillators due to Power Supply Noise. IEICE Transactions on Electronics, 2009, E92-C, 973-975.	0.3	1
103	A CMOS broadband frequency synthesizer for DVB-C receiver. Analog Integrated Circuits and Signal Processing, 2007, 52, 109-115.	0.9	0