Jeeson Kim

List of Publications by Year
in descending order

15 papers	364 citations	1162889 8 h-index	1372474 10 g-index
15 all docs	15 docs citations	15 times ranked	570 citing authors

#	Article	IF	Citations
1	Hardware-Efficient Emulation of Leaky Integrate-and-Fire Model Using Template-Scaling-Based Exponential Function Approximation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 350-362.	3.5	10
2	Self-rectifying resistive memory in passive crossbar arrays. Nature Communications, 2021, 12, 2968.	5.8	53
3	Exploiting machine learning for bestowing intelligence to microfluidics. Biosensors and Bioelectronics, 2021, 194, 113666.	5.3	31
4	TS-EFA: Resource-efficient High-precision Approximation of Exponential Functions Based on Template-scaling Method. , 2020, , .		5
5	Optimal Distribution of Spiking Neurons Over Multicore Neuromorphic Processors. IEEE Access, 2020, 8, 69426-69437.	2.6	4
6	FPGA implementation of sequence-to-sequence predicting spiking neural networks. , 2020, , .		0
7	Combination-Encoding Content-Addressable Memory With High Content Density. IEEE Access, 2019, 7, 137620-137628.	2.6	2
8	Nano-Intrinsic True Random Number Generation: A Device to Data Study. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2615-2626.	3.5	19
9	Hardware-intrinsic security primitives enabled by analogue state and nonlinear conductance variations in integrated memristors. Nature Electronics, 2018, 1, 197-202.	13.1	148
10	A Physical Unclonable Function With Redox-Based Nanoionic Resistive Memory. IEEE Transactions on Information Forensics and Security, 2018, 13, 437-448.	4.5	24
11	Predictive Analysis of 3D ReRAM-Based PUF for Securing the Internet of Things. , 2018, , .		4
12	Transparent amorphous strontium titanate resistive memories with transient photo-response. Nanoscale, 2017, 9, 14690-14702.	2.8	18
13	Microstructure and dynamics of vacancy-induced nanofilamentary switching network in donor doped SrTiO$_{3−x}$ memristors. Nanotechnology, 2016, 27, 505210.	1.3	39
14	Static leakage control in null convention logic standard cells in 28 nm UTBB-FDSOI CMOS. , 2015, , .		2
15	Area performance tradeoffs in NCL multipliers using two-dimensional pipelining. , 2015, , .		5