JÃ¼rgen Teich

List of Publications by Year
in descending order

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122	2,066	623734	414414
papers	citations	14	32
		h-index	g-index

124	124	124	1207
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Design and Evaluation of a Tunable PUF Architecture for FPGAs. ACM Transactions on Reconfigurable Technology and Systems, 2022, 15, 1-27.	2.5	0
2	Task Migration Policy for Thermal-Aware Dynamic Performance Optimization in Many-Core Systems. IEEE Access, 2022, 10, 33787-33802.	4.2	2
3	Design and error analysis of accuracy-configurable sequential multipliers via segmented carry chains. IT - Information Technology, 2022, .	0.9	0
4	Precision- and Accuracy-Reconfigurable Processor Architecturesâ€"An Overview. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2661-2666.	3.0	4
5	Adaptive Predictive Power Management for Mobile LTE Devices. IEEE Transactions on Mobile Computing, 2021, 20, 2518-2535.	5.8	5
6	*â€Predictable MPSoC execution of realâ€time control applications using invasive computing. Concurrency Computation Practice and Experience, 2021, 33, e5149.	2.2	1
7	Providing Tamper-Secure SoC Updates Through Reconfigurable Hardware. Lecture Notes in Computer Science, 2021, , 242-253.	1.3	2
8	Symbolic Loop Compilation for Tightly Coupled Processor Arrays. Transactions on Embedded Computing Systems, 2021, 20, 1-31.	2.9	1
9	Domain-Adaptive Soft Real-Time Hybrid Application Mapping for MPSoCs. , 2021, , .		1
10	Open Source Hardware. Computer, 2021, 54, 111-115.	1.1	3
11	Efficient Symbolic Routing Encoding for In-vehicle Network Optimization. Communications in Computer and Information Science, 2021, , 173-199.	0.5	0
12	Efficient Computation of Probabilistic Dominance in Multi-objective Optimization. ACM Transactions on Evolutionary Learning, 2021, 1, 1-26.	3.5	2
13	LION. , 2021, , .		0
14	Hybrid Application Mapping for Composable Many-Core Systems: Overview and Future Perspective. Journal of Low Power Electronics and Applications, 2020, 10, 38.	2.0	7
15	ExaStencils: Advanced Multigrid Solver Generation. Lecture Notes in Computational Science and Engineering, 2020, , 405-452.	0.3	10
16	Secure Boot from Non-Volatile Memory for Programmable SoC Architectures. , 2020, , .		7
17	A runtime system for finite element methods in a partitioned global address space. , 2020, , .		2
18	Probabilistic Error Propagation through Approximated Boolean Networks. , 2020, , .		8

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19	IGOR, Get Me the Optimum! Prioritizing Important Design Decisions During the DSE of Embedded Systems. Transactions on Embedded Computing Systems, 2019, 18, 1-22.	2.9	6
20	Polyhedral fragments. , 2019, , .		1
21	Conference Reports: Recap of DATE 2019 in Florence, Italy. IEEE Design and Test, 2019, 36, 59-61.	1.2	0
22	On the Analytic Evaluation of Schedules via Max-Plus Algebra for DSE of Multi-Core Architectures. , 2019, , .		1
23	Hard real-time application mapping reconfiguration for NoC-based many-core systems. Real-Time Systems, 2019, 55, 433-469.	1.3	14
24	Anytime instructions for programmable accuracy floating-point arithmetic. , 2019, , .		3
25	Efficient Mapping of Streaming Applications for Image Processing on Graphics Cards. Lecture Notes in Computer Science, 2019, , 1-20.	1.3	0
26	Variety-aware Routing Encoding for Efficient Design Space Exploration of Automotive Communication Networks. , 2019, , .		2
27	DSL-Based Acceleration of Automotive Environment Perception and Mapping Algorithms for Embedded CPUs, GPUs, and FPGAs. Lecture Notes in Computer Science, 2019, , 71-86.	1.3	0
28	Thermally Composable Hybrid Application Mapping for Real-Time Applications in Heterogeneous Many-Core Systems. , 2019, , .		6
29	Time-Critical Systems Design: A Survey. IEEE Design and Test, 2018, 35, 8-26.	1.2	19
30	Cell-based update algorithm for occupancy grid maps and hybrid map for ADAS on embedded GPUs. , 2018, , .		4
31	Guest Editorsâ€™ Introduction: Special Issue on Time-Critical Systems Design. IEEE Design and Test, 2018, 35, 5-7.	1.2	0
32	Symbolic Multi-Level Loop Mapping of Loop Programs for Massively Parallel Processor Arrays. Transactions on Embedded Computing Systems, 2018, 17, 1-27.	2.9	2
33	Efficient Arithmetic Error Rate Calculus for Visibility Reduced Approximate Adders. IEEE Embedded Systems Letters, 2018, 10, 37-40.	1.9	6
34	Reconfigurable Hardware Generation of Multigrid Solvers with Conjugate Gradient Coarse-Grid Solution. Parallel Processing Letters, 2018, 28, 1850016.	0.6	4
35	Model-Based Design Automation of Hardware/Software Co-Designs for Xilinx Zynq PSoCs. , 2018, , .		6
36	Path Planning for Highly Automated Driving on Embedded GPUs. Journal of Low Power Electronics and Applications, 2018, 8, 35.	2.0	10

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37	Can Approximate Computing Reduce Power Consumption on FPGAs?. , 2018, , .		4
38	AConFPGA: A Multiple-Output Boolean Function Approximation DSE Technique Targeting FPGAs. , 2018, , .		1
39	A Design-Time/Run-Time Application Mapping Methodology for Predictable Execution Time in MPSoCs. Transactions on Embedded Computing Systems, 2018, 17, 1-25.	2.9	11
40	Automating the Development of High-Performance Multigrid Solvers. Proceedings of the IEEE, 2018, 106, 1969-1984.	21.3	4
41	Reinforcement Learning for Power-Efficient Grant Prediction in LTE. , 2018, , .		3
42	A predictive dynamic power management for LTE-Advanced mobile devices. , 2018, , .		9
43	Automatic Optimization of Redundant Message Routings in Automotive Networks. , 2018, , .		12
44	Symmetry-Eliminating Design Space Exploration for Hybrid Application Mapping on Many-Core Architectures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 297-310.	2.7	24
45	Base Algorithms of Environment Maps and Efficient Occupancy Grid Mapping on Embedded GPUs. , 2018, , .		1
46	Automatic operating point distillation for hybrid mapping methodologies. , 2017, , .		8
47	Optimizing Message Routing and Scheduling in Automotive Mixed-Criticality Time-Triggered Networks. , 2017, , .		40
48	Exploiting Predictability in Dynamic Network Communication for Power-Efficient Data Transmission in LTE Radio Systems. , 2017, , .		4
49	Predictable run-time mapping reconfiguration for real-time applications on many-core systems. , 2017, , .		8
50	Optimizing scrubbing by netlist analysis for FPGA configuration bit classification and floorplanning. The Integration VLSI Journal, 2017, 59, 98-108.	2.1	3
51	Power Density-Aware Resource Management for Heterogeneous Tiled Multicores. IEEE Transactions on Computers, 2017, 66, 488-501.	3.4	54
52	High-Level Synthesis for Hardware/Software Co-Design of Distributed Smart Camera Systems. , 2017, , .		7
53	Generating FPGA-based image processing accelerators with Hipacc: (Invited paper). , 2017, , .		18
54	A reconfigurable memory architecture for system integration of coarse-grained reconfigurable arrays. , 2017, , .		2

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55	Auto-vectorization for image processing DSLs. , 2017, , .		6
56	Towards the co-evolution of industrial products and its production systems by combining models from development and hardware/software deployment in cyber-physical systems. Production Engineering, 2017, 11, 687-694.	2.3	13
57	Reconfigurable Buffer Structures forÂCoarse-Grained Reconfigurable Arrays. IFIP Advances in Information and Communication Technology, 2017, , 218-229.	0.7	0
58	Invasive computing for timing-predictable stream processing on MPSoCs. IT - Information Technology, 2016, 58, 267-280.	0.9	5
59	ReOrder: Runtime datapath generation for high-throughput multi-stream processing. , 2016, , .		0
60	Modeling, programming and performance analysis of automotive environment map representations on embedded GPUs. , 2016, , .		4
61	Language and Compilation of Parallel Programs for *-Predictable MPSoC Execution Using Invasive Computing. , 2016, , .		14
62	FAU: Fast and error-optimized approximate adder units on LUT-Based FPGAs. , 2016, , .		16
63	A LUT-Based Approximate Adder. , 2016, , .		14
64	Systems of Partial Differential Equations in ExaSlang. Lecture Notes in Computational Science and Engineering, 2016, , 47-67.	0.3	5
65	Modulo scheduling of symbolically tiled loops for tightly coupled processor arrays. , 2016, , .		4
66	HIPA^{cc}: A Domain-Specific Language and Compiler for Image Processing. IEEE Transactions on Parallel and Distributed Systems, 2016, 27, 210-224.	5.6	85
67	Formal Analysis of the Startup Delay of SOME/IP Service Discovery. , 2015, , .		11
68	Runtime Adaptation of Application Execution under Thermal and Power Constraints in Massively Parallel Processor Arrays. , 2015, , .		4
69	A co-design approach for fault-tolerant loop execution on Coarse-Grained Reconfigurable Arrays. , 2015, , .		7
70	Compact Code Generation and Throughput Optimization for Coarse-Grained Reconfigurable Arrays. , 2015, , 167-206.		2
71	MAESTROâ€" Holistic Actor-Oriented Modeling of Nonfunctional Properties and Firmware Behavior for MPSoCs. ACM Transactions on Design Automation of Electronic Systems, 2014, 19, 1-26.	2.6	19
72	Minimizing Scrubbing Effort through Automatic Netlist Partitioning and Floorplanning. , 2014, , .		5

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73	Self-adaptive harris corner detector on heterogeneous many-core processor. , 2014, , .		1
74	Towards scalable symbolic routing for multi-objective networked embedded system design and optimization. , 2014, , .		11
75	DAARM. , 2014, , .		45
76	End-to-end power estimation for heterogeneous cellular LTE SoCs in early design phases. , 2014, , .		10
77	An Evaluation of Domain-Specific Language Technologies for Code Generation. , 2014, , .		12
78	A self-propagating wakeup mechanism for point-to-point networks with partial network support. , 2014, , .		1
79	DPSK modulated wakeup mechanism for point-to-point networks with partial network support. , 2014, , .		0
80	A self-propagating wakeup mechanism for point-to-point networks with partial network support. , 2014, , .		4
81	Towards a performance-portable description of geometric multigrid algorithms using a domain-specific language. Journal of Parallel and Distributed Computing, 2014, 74, 3191-3201.	4.1	12
82	Code generation for embedded heterogeneous architectures on android. , 2014, , .		5
83	Symbolic Mapping of Loop Programs onto Processor Arrays. Journal of Signal Processing Systems, 2014, 77, 31-59.	2.1	20
84	Compact Code Generation for Tightly-Coupled Processor Arrays. Journal of Signal Processing Systems, 2014, 77, 5-29.	2.1	10
85	ExaSlang: A Domain-Specific Language for Highly Scalable Multigrid Solvers. , 2014, , .		28
86	Application-driven reconfiguration of shared resources for timing predictability of MPSoC platforms. , 2014, , .		4
87	ExaStencils: Advanced Stencil-Code Engineering. Lecture Notes in Computer Science, 2014, , 553-564.	1.3	30
88	Code generation for embedded heterogeneous architectures on android. , 2014, , .		8
89	Loop program mapping and compact code generation for programmable hardware accelerators. , 2013, , .		8
90	System integration of tightly-coupled processor arrays using reconfigurable buffer structures. , 2013, , .		11

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91	Symbolic parallelization of loop programs for massively parallel processor arrays. , 2013, , .		18
92	Power Management Strategies for Serial RapidIO Endpoints in FPGAs. , 2012, , .		1
93	FPGA-based testbed for timing behavior evaluation of the Controller Area Network (CAN). , 2012, , .		1
94	On-the-fly Composition of FPGA-Based SQL Query Accelerators Using a Partially Reconfigurable Module Library. , 2012, , .		47
95	Towards Domain-Specific Computing for Stencil Codes in HPC. , 2012, , .		23
96	Model-Based Virtual Prototype Acceleration. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1572-1585.	2.7	4
97	Approximate time functional simulation of resource-aware programming concepts for heterogeneous MPSoCs. , 2012, , .		6
98	Generating Device-specific GPU Code for Local Operators in Medical Imaging. , 2012, , .		36
99	Hardware/Software Codesign: The Past, the Present, and Predicting the Future. Proceedings of the IEEE, 2012, 100, 1411-1430.	21.3	211
100	Decentralized dynamic resource management support for massively parallel processor arrays. , 2011, , .		20
101	Stress-Aware Module Placement on Reconfigurable Devices. , 2011, , .		20
102	Calibration and validation of software performance models for pedestrian detection systems. , 2011, , .		2
103	An FPGA implementation of a threat-based strategy for Connect6. , 2011, , .		1
104	Opt4J. , 2011, , .		148
105	Towards Symbolic Run-Time Reconfiguration in Tightly-Coupled Processor Arrays. , 2011, , .		4
106	Invasive Computing: An Overview. , 2011, , 241-268.		95
107	A system-level synthesis approach from formal application models to generic bus-based MPSoCs. , 2010, , .		6
108	FSM-controlled architectures for linear invasion. , 2009, , .		5

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109	Combined system synthesis and communication architecture exploration for MPSoCs. , 2009, , .		35
110	Self-organizing Bandwidth Sharing in Priority-Based Medium Access. , 2009, , .		5
111	Power-Efficient Reconfiguration Control in Coarse-Grained Dynamically Reconfigurable Architectures. Journal of Low Power Electronics, 2009, 5, 96-105.	0.6	15
112	Power Signature Watermarking of IP Cores for FPGAs. Journal of Signal Processing Systems, 2008, 51, 123-136.	2.1	72
113	SPP1148 booth: Coarse-grained reconfiguration. , 2008, , .		0
114	PARO: Synthesis of Hardware Accelerators for Multi-dimensional Dataflow-Intensive Applications. Lecture Notes in Computer Science, 2008, , 287-293.	1.3	43
115	Actor-Oriented Modeling and Simulation of Sliding Window Image Processing Algorithms. , 2007, , .		4
116	SAT-decoding in evolutionary algorithms for discrete constrained optimization problems. , 2007, , .		32
117	A highly parameterizable parallel processor array architecture. , 2006, , .		52
118	Hardware Cost Analysis for Weakly Programmable Processor Arrays. , 2006, , .		4
119	A Design Methodology for Hardware Acceleration of Adaptive Filter Algorithms in Image Processing. , 2006, , .		22
120	Mapping a class of dependence algorithms to coarse-grained reconfigurable arrays: architectural parameters and methodology. International Journal of Embedded Systems, 2006, 2, 114.	0.3	17
121	Pareto-Front Exploration with Uncertain Objectives. Lecture Notes in Computer Science, 2001, , 314-328.	1.3	162
122	System-Level Synthesis Using Evolutionary Algorithms. Design Automation for Embedded Systems, 1998, 3, 23-58.	1.0	157