

Zhang-ming Zhu

List of Publications by Year in descending order

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all docs

162
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times ranked

1358
citing authors

#	ARTICLE	IF	CITATIONS
1	V _{CM} -based monotonic capacitor switching scheme for SAR ADC. Electronics Letters, 2013, 49, 327-329.	0.5	136
2	A 0.6-V 38-nW 9.4-ENOB 20-kS/s SAR ADC in 0.18- μm CMOS for Medical Implant Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2167-2176.	3.5	109
3	A 12-Bit 10 MS/s SAR ADC With High Linearity and Energy-Efficient Switching. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1616-1627.	3.5	90
4	A Second-Order Noise-Shaping SAR ADC With Passive Integrator and Tri-Level Voting. IEEE Journal of Solid-State Circuits, 2019, 54, 1636-1647.	3.5	75
5	A 6-to-10-Bit 0.5 V-to-0.9 V Reconfigurable 2 MS/s Power Scalable SAR ADC in 0.18 μm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 689-696.	3.5	65
6	A Reconfigurable 10-to-12-b 80-to-20-MS/s Bandwidth Scalable SAR ADC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 51-60.	3.5	54
7	Electrical Modeling and Characterization of Shield Differential Through-Silicon Vias. IEEE Transactions on Electron Devices, 2015, 62, 1544-1552.	1.6	52
8	Ultra-Compact TSV-Based L-C Low-Pass Filter With Stopband Up to 40 GHz for Microwave Application. IEEE Transactions on Microwave Theory and Techniques, 2019, 67, 738-745.	2.9	49
9	Metal Proportion Optimization of Annular Through-Silicon via Considering Temperature and Keep-Out Zone. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2015, 5, 1093-1099.	1.4	44
10	A 9.1ENOB 200MS/s Asynchronous SAR ADC With Hybrid Single-Ended/Differential DAC in 55-nm CMOS for Image Sensing Signals. IEEE Sensors Journal, 2018, 18, 7130-7140.	2.4	44
11	A 19-nW 0.7-V CMOS Voltage Reference With No Amplifiers and No Clock Circuits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 830-834.	2.2	42
12	An Effective Approach of Reducing the Keep-Out-Zone Induced by Coaxial Through-Silicon-Via. IEEE Transactions on Electron Devices, 2014, 61, 2928-2934.	1.6	40
13	Utilization of Negative-Capacitance FETs to Boost Analog Circuit Performances. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2855-2860.	2.1	40
14	Influence of Body Effect on Sample-and-Hold Circuit Design Using Negative Capacitance FET. IEEE Transactions on Electron Devices, 2018, 65, 3909-3914.	1.6	38
15	Wideband Substrate Integrated Waveguide Bandpass Filter Based on 3-D ICs. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 728-735.	1.4	36
16	Modeling and Optimization of Multiground TSVs for Signals Shield in 3-D ICs. IEEE Transactions on Electromagnetic Compatibility, 2017, 59, 461-467.	1.4	34
17	A Sub-200nW All-in-One Bandgap Voltage and Current Reference Without Amplifiers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 121-125.	2.2	34
18	Compact Bandpass Filter and Diplexer With Wide-Stopband Suppression Based on Balanced Substrate-Integrated Waveguide. IEEE Transactions on Microwave Theory and Techniques, 2021, 69, 54-64.	2.9	33

#	ARTICLE	IF	CITATIONS
19	A 66-dB Linear Dynamic Range, 100-dB Ω Transimpedance Gain TIA With High-Speed PDSH for LiDAR. IEEE Transactions on Instrumentation and Measurement, 2020, 69, 1020-1028.	2.4	31
20	A 0.55-V, 28-ppm/ $^{\circ}$ C, 83-nW CMOS Sub-BGR With UltraLow Power Curvature Compensation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 95-106.	3.5	30
21	A 1.4-mW 10-Bit 150-MS/s SAR ADC With Nonbinary Split Capacitive DAC in 65-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1524-1528.	2.2	29
22	A 77-dB Dynamic Range Low-Power Variable-Gain Transimpedance Amplifier for Linear LADAR. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 171-175.	2.2	28
23	A 1.2-V 2.41-GHz Three-Stage CMOS OTA With Efficient Frequency Compensation Technique. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 20-30.	3.5	28
24	An 8-ch LIDAR Receiver Based on TDC With Multi-Interval Detection and Real-Time \ln -Situ Calibration. IEEE Transactions on Instrumentation and Measurement, 2020, 69, 5081-5090.	2.4	28
25	A Low Walk Error Analog Front-End Circuit With Intensity Compensation for Direct ToF LiDAR. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4309-4321.	3.5	28
26	A Linear Dynamic Range Receiver With Timing Discrimination for Pulsed TOF Imaging LADAR Application. IEEE Transactions on Instrumentation and Measurement, 2018, 67, 2684-2691.	2.4	27
27	A 60-m Range 6.16-mW Laser-Power Linear-Mode LiDAR System With Multiplex ADC/TDC in 65-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 753-764.	3.5	27
28	Mismatch of Ferroelectric Film on Negative Capacitance FETs Performance. IEEE Transactions on Electron Devices, 2020, 67, 1297-1304.	1.6	26
29	High Sensitivity and Wide Dynamic Range Analog Front-End Circuits for Pulsed TOF 4-D Imaging LADAR Receiver. IEEE Sensors Journal, 2018, 18, 3114-3124.	2.4	24
30	A Two-Step ADC With a Continuous-Time SAR-Based First Stage. IEEE Journal of Solid-State Circuits, 2019, 54, 3375-3385.	3.5	24
31	A 7-bit 900-MS/s 2-Then-3-bit/cycle SAR ADC With Background Offset Calibration. IEEE Journal of Solid-State Circuits, 2020, 55, 3051-3063.	3.5	24
32	Electrical Modeling and Analysis of Differential Dielectric-Cavity Through-Silicon via Array. IEEE Microwave and Wireless Components Letters, 2017, 27, 618-620.	2.0	23
33	A $64.8\text{-}\mu\text{W}$ > 2.2 G Ω DC \leftrightarrow AC Configurable CMOS Front-End IC for Wearable ECG Monitoring. IEEE Sensors Journal, 2018, 18, 3400-3409.	2.4	22
34	A Broadband Planar Balun Using Aperture-Coupled Microstrip-to-SIW Transition. IEEE Microwave and Wireless Components Letters, 2019, 29, 532-534.	2.0	22
35	A 10-Bit 600-MS/s Time-Interleaved SAR ADC With Interpolation-Based Timing Skew Calibration. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 16-20.	2.2	22
36	A 0.5-V power-efficient low-noise CMOS instrumentation amplifier for wireless biosensor. Microelectronics Journal, 2016, 51, 30-37.	1.1	21

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37	Low-Power Single-Ended SAR ADC Using Symmetrical DAC Switching for Image Sensors With Passive CDS and PGA Technique. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 2378-2388.	3.5	21
38	A 10-Bit 5 MS/s VCO-SAR ADC in 0.18- μm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 26-30.	2.2	21
39	Trade-off between energy and linearity switching scheme for SAR ADC. Analog Integrated Circuits and Signal Processing, 2016, 86, 121-125.	0.9	20
40	Self-Compensating OCP Control Scheme for Primary-Side Controlled Flyback AC/DC Converters. IEEE Transactions on Power Electronics, 2017, 32, 3673-3682.	5.4	20
41	A transconductance-enhancement cascode Miller compensation for low-power multistage amplifiers. Microelectronics Journal, 2018, 73, 94-100.	1.1	20
42	Wideband Fourth-Harmonic Mixer Operated at 325-500 GHz. IEEE Microwave and Wireless Components Letters, 2018, 28, 242-244.	2.0	19
43	A 32- μm 32-Pixel Flash LiDAR Sensor With Noise Filtering for High-Background Noise Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 645-656.	3.5	19
44	A 10-Bit Self-Clocked SAR ADC With Enhanced Energy Efficiency for Multi-Sensor Applications. IEEE Sensors Journal, 2018, 18, 4223-4233.	2.4	18
45	3-D Compact 3-dB Branch-Line Directional Couplers Based on Through-Silicon Via Technology for Millimeter-Wave Applications. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 1855-1862.	1.4	18
46	A 10-kS/s 625-Hz-Bandwidth 65-dB SNDR Second-Order Noise-Shaping SAR ADC for Biomedical Sensor Applications. IEEE Sensors Journal, 2020, 20, 13881-13891.	2.4	18
47	A 12-Bit 100-MS/s Pipelined-SAR ADC With PVT-Insensitive and Gain-Folding Dynamic Amplifier. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 2602-2611.	3.5	18
48	A CMOS transimpedance amplifier with high gain and wide dynamic range for optical fiber sensing system. Optik, 2015, 126, 1389-1393.	1.4	17
49	A Routing Aggregation for Load Balancing Network-on-Chip. Journal of Circuits, Systems and Computers, 2015, 24, 1550137.	1.0	17
50	A background fast convergence algorithm for timing skew in time-interleaved ADCs. Microelectronics Journal, 2016, 47, 45-52.	1.1	17
51	High-Frequency Electrical Model of Through-Silicon Vias for 3-D Integrated Circuits Considering Eddy Current and Proximity Effects. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2017, 7, 2036-2044.	1.4	17
52	A Linear-Array Receiver Analog Front-End Circuit for Rotating Scanner LiDAR Application. IEEE Sensors Journal, 2019, 19, 5053-5061.	2.4	17
53	A High Linearity TDC With a United-Reference Fractional Counter for LiDAR. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 564-572.	3.5	17
54	Low-Loss Air-Cavity Through-Silicon Vias (TSVs) for High Speed Three-Dimensional Integrated Circuits (3-D ICs). IEEE Microwave and Wireless Components Letters, 2016, 26, 89-91.	2.0	16

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55	A P&O MPPT With a Novel Analog Power-Detector for WSNs Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1680-1684.	2.2	16
56	A 2nd-Order Noise-Shaping SAR ADC With Lossless Dynamic Amplifier Assisted Integrator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1819-1823.	2.2	16
57	Wideband Electromagnetic Model and Analysis of Shielded-Pair Through-Silicon Vias. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018, 8, 473-481.	1.4	15
58	A 10-bit 120-MS/s SAR ADC With Reference Ripple Cancellation Technique. IEEE Journal of Solid-State Circuits, 2020, 55, 680-692.	3.5	15
59	A Robust Bio-IA With Digitally Controlled DC-Servo Loop and Improved Pseudo-Resistor. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 440-444.	2.2	15
60	A CMOS Peak Detect and Hold Circuit With Auto-Adjust Charging Current for NS-Scale Pulse ToF Lidar Application. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4409-4419.	3.5	15
61	A 0.6 μ s 100kS/s 8 \times 10 μ s resolution configurable SAR ADC in 0.18 μ m CMOS. Analog Integrated Circuits and Signal Processing, 2013, 75, 335-342.	0.9	14
62	Wideband Electromagnetic Modeling of Coaxial-Annular Through-Silicon Vias. IEEE Transactions on Electromagnetic Compatibility, 2018, 60, 1915-1922.	1.4	14
63	A 5-GHz Low-Power Low-Noise Integer-N Digital Subsampling PLL With SAR ADC PD. IEEE Transactions on Microwave Theory and Techniques, 2018, 66, 4078-4087.	2.9	14
64	A Self-Powered Rectifier-Less Synchronized Switch Harvesting on Inductor Interface Circuit for Piezoelectric Energy Harvesting. IEEE Transactions on Power Electronics, 2021, 36, 9149-9159.	5.4	14
65	A fair arbitration for Network-on-Chip routing with odd-even turn model. Microelectronics Journal, 2017, 64, 1-8.	1.1	13
66	An Adaptive High-Precision OCP Control Scheme for Flyback AC/DC Converters. IEEE Transactions on Power Electronics, 2017, 32, 8969-8973.	5.4	13
67	An asynchronous 12-bit 50MS/s rail-to-rail Pipeline-SAR ADC in 0.18 μ m CMOS. Microelectronics Journal, 2016, 52, 23-30.	1.1	12
68	A high accuracy CMOS subthreshold voltage reference with offset cancellation and thermal compensation. Microelectronics Journal, 2017, 60, 102-108.	1.1	12
69	A Capacitor-Free Control Scheme for a Primary-Side Controlled Flyback Converter. IEEE Transactions on Power Electronics, 2020, 35, 9482-9493.	5.4	12
70	An 8-Bit 2.1-mW 350-MS/s SAR ADC With 1.5 b/cycle Redundancy in 65-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2307-2311.	2.2	12
71	An 8/10 bit 200/100MS/s configurable asynchronous SAR ADC. Analog Integrated Circuits and Signal Processing, 2013, 77, 249-255.	0.9	11
72	A 10-bit 100-MS/s 5.23-mW SAR ADC in 0.18 μ m CMOS. Microelectronics Journal, 2018, 78, 63-72.	1.1	11

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73	Performance Enhancement of Broadband Circularly Polarized Slot-Loaded Microstrip Antenna Using Parasitic Elements. <i>IEEE Antennas and Wireless Propagation Letters</i> , 2021, 20, 2255-2259.	2.4	11
74	A single-channel 8-bit 660MS/s asynchronous SAR ADC with pre-settling procedure in 65nm CMOS. <i>Microelectronics Journal</i> , 2014, 45, 880-885.	1.1	10
75	Energy-efficient common-mode voltage switching scheme for SAR ADCs. <i>Analog Integrated Circuits and Signal Processing</i> , 2016, 89, 499-506.	0.9	10
76	A 10bit 20kS/s 17.7nW 9.1ENOB reference-insensitive SAR ADC in 0.18µm CMOS. <i>Microelectronics Journal</i> , 2018, 73, 24-29.	1.1	10
77	High energy-efficient partial floating capacitor array DAC scheme for SAR ADCs. <i>Analog Integrated Circuits and Signal Processing</i> , 2018, 94, 171-175.	0.9	10
78	A highly energy-efficient, highly area-efficient capacitance multiplexing switching scheme for SAR ADC. <i>Analog Integrated Circuits and Signal Processing</i> , 2018, 96, 207-215.	0.9	10
79	A 12-GHz Wideband Fractional-N PLL With Robust VCO in 65-nm CMOS. <i>IEEE Microwave and Wireless Components Letters</i> , 2019, 29, 397-399.	2.0	10
80	Area-Efficient Extended 3-D Inductor Based on TSV Technology for RF Applications. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2021, 29, 287-296.	2.1	10
81	An ultra-low-voltage self-powered energy harvesting rectifier with digital switch control. <i>IEICE Electronics Express</i> , 2015, 12, 20140921-20140921.	0.3	9
82	A background digital calibration of split-capacitor 16-bit SAR ADC with sub-binary architecture. <i>Microelectronics Journal</i> , 2015, 46, 795-800.	1.1	9
83	An 8-Bit 0.333GS/s Configurable Time-Interleaved SAR ADC in 65-nm CMOS. <i>Journal of Circuits, Systems and Computers</i> , 2015, 24, 1550093.	1.0	9
84	A 0.6 V 31 nW 25 ppm/°C MOSFET-only sub-threshold voltage reference. <i>Microelectronics Journal</i> , 2017, 66, 25-30.	1.1	9
85	High-Frequency Electrical Modeling and Characterization of Differential TSVs for 3-D Integration Applications. <i>IEEE Microwave and Wireless Components Letters</i> , 2017, 27, 721-723.	2.0	9
86	A 42ppm/°C 0.7V 47nW Low-Complexity All-MOSFET Sub-Threshold Voltage Reference. <i>Journal of Circuits, Systems and Computers</i> , 2018, 27, 1850105.	1.0	9
87	Low-Noise Fractional-N PLL With a High-Precision Phase Control in the Phase Synchronization of Multichips. <i>IEEE Microwave and Wireless Components Letters</i> , 2018, 28, 702-704.	2.0	9
88	A Dual-Supply Two-Stage CMOS Op-amp for High-Speed Pipeline ADCs Application. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2020, 67, 650-654.	2.2	9
89	An 11-bit 100-MS/s Pipelined-SAR ADC Reusing PVT-Stabilized Dynamic Comparator in 65-nm CMOS. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2020, 67, 1174-1178.	2.2	9
90	A Conversion Mode Reconfigurable SAR ADC for Multistandard Systems. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2021, 29, 895-903.	2.1	9

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91	High efficiency two-step capacitor switching scheme for SAR ADC. Analog Integrated Circuits and Signal Processing, 2016, 86, 127-131.	0.9	8
92	A 30-W 90% Efficiency Dual-Mode Controlled DC-DC Controller With Power Over Ethernet Interface for Power Device. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1943-1953.	2.1	8
93	A linear and wide dynamic range transimpedance amplifier with adaptive gain control technique. Analog Integrated Circuits and Signal Processing, 2017, 90, 217-226.	0.9	8
94	Energy-Efficient and Area-Saving Asymmetric Capacitor Switching Scheme for SAR ADCs. Journal of Circuits, Systems and Computers, 2018, 27, 1850109.	1.0	8
95	Average Inductor Current Measure and Control Strategy for Multimode Primary-Side Flyback Converters. IEEE Transactions on Power Electronics, 2020, 35, 13096-13103.	5.4	8
96	A 12-bit 50MS/s zero-crossing-based two-stage pipelined SAR ADC in 0.18 μ m CMOS. Microelectronics Journal, 2016, 57, 26-33.	1.1	7
97	A 7b 2.6mW 900MS/s Nonbinary 2-then-3b/cycle SAR ADC with Background Offset Calibration. , 2019, , .		7
98	High Input Impedance Low-Noise CMOS Analog Frontend IC for Wearable Electrocardiogram Monitoring. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1169-1173.	2.2	7
99	A 3.03 μ W 10-BIT 200 KS/s SAR ADC IN 0.18 μ M CMOS. Journal of Circuits, Systems and Computers, 2013, 22, 1350026.	1.0	6
100	A 10-bit 300-MS/s asynchronous SAR ADC with strategy of optimizing settling time for capacitive DAC in 65nm CMOS. Microelectronics Journal, 2015, 46, 988-995.	1.1	6
101	Energy-efficient and two-step structure switching scheme based on reference-free for SAR ADC. Analog Integrated Circuits and Signal Processing, 2019, 99, 209-218.	0.9	6
102	Electromagnetic modeling and analysis of the tapered differential through glass vias. Microelectronics Journal, 2019, 83, 27-31.	1.1	6
103	A novel split capacitor array switching scheme with proportional coefficient for SAR ADC. Analog Integrated Circuits and Signal Processing, 2019, 98, 597-605.	0.9	6
104	Compact and Physics-Based Modeling of 3-D Inductor Based on Through Silicon Via. IEEE Electron Device Letters, 2021, 42, 1559-1562.	2.2	6
105	Low walk error multi-stage cascade comparator for TOF LiDAR application. Microelectronics Journal, 2021, 116, 105194.	1.1	6
106	A 26 μ W 31 GHz Linearized Wideband CMOS LNA Using Post-Distortion Technique. IEEE Microwave and Wireless Components Letters, 2022, 32, 1087-1090.	2.0	6
107	A Background Timing Skew Calibration Technique in Time-Interleaved ADCs With Second Order Compensation. , 2018, , .		5
108	A congestion-aware OE router employing fair arbitration for network-on-chip. Journal of Semiconductors, 2018, 39, 125006.	2.0	5

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109	A 0.6-V 9-bit 1-MS/s Charging Sharing SAR ADC With Judging-Window Switching Logic and Independent Reset Comparator for Power-Effective Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1750-1754.	2.2	5
110	Millimeter-Wave Antenna-in-Package Applications Based on D263T Glass Substrate. IEEE Access, 2020, 8, 67921-67928.	2.6	5
111	A <sc>30â€GHz</sc> lowâ€power <sc>CMOS LNA</sc> for <sc>5G</sc> communication systems. Microwave and Optical Technology Letters, 2021, 63, 746-752.	0.9	5
112	A 2.6ÂĈ, 1.4 Î¼Vrms current-reuse instrumentation amplifier for wearable electrocardiogram monitoring. Microelectronics Journal, 2021, 107, 104940.	1.1	5
113	A TD-ADC for IR-UWB Radars With Equivalent Sampling Technology and 8-GS/s Effective Sampling Rate. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 888-892.	2.2	5
114	Radio frequency analog-to-digital converters: Systems and circuits review. Microelectronics Journal, 2022, 119, 105331.	1.1	5
115	Performance analysis of singleâ€walled carbon nanotube bundle interconnects for threeâ€dimensional integration applications. Micro and Nano Letters, 2013, 8, 56-58.	0.6	4
116	A 10-GS/s 6-Bit Track-and-Hold Amplifier for Time-Interleaved SAR ADCs in 65-nm CMOS. Journal of Circuits, Systems and Computers, 2016, 25, 1650084.	1.0	4
117	High-resolution 1 MS/s sub-2 radix split-capacitor SAR ADC. Journal of Semiconductors, 2017, 38, 105008.	2.0	4
118	Inductance Modeling of Interconnections in 3-D Stacked-Chip Packaging. IEEE Microwave and Wireless Components Letters, 2018, 28, 281-283.	2.0	4
119	A Multiplexing DAPD Technique for Fast-Locking and Charge Pumps Calibration in PLLs. IEEE Microwave and Wireless Components Letters, 2019, 29, 535-537.	2.0	4
120	A Compact High-Performance Programmable-Gain Analog Front End for HomePlug AV2 Communication in 0.18- μm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2858-2870.	3.5	4
121	A 16-Channel Analog CMOS SiPM With On-Chip Front-End for D-ToF LiDAR. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2376-2386.	3.5	4
122	A low-distortion CMOS analogue voltage follower for high-speed ADCs. Microelectronics Journal, 2016, 54, 67-71.	1.1	3
123	A dynamic task mapping algorithm for SDNoC. Microelectronics Journal, 2017, 63, 58-65.	1.1	3
124	A High Energy Efficiency and Low Common-Mode Voltage Variation Switching Scheme for SAR ADCs. Journal of Circuits, Systems and Computers, 2018, 27, 1850010.	1.0	3
125	Two-step switching scheme for SAR ADC with high energy efficiency. Analog Integrated Circuits and Signal Processing, 2018, 96, 189-195.	0.9	3
126	An 8-bit, 8-GS/s Equivalent Sampling Time Domain Analog-to-digital Converter. , 2019, , .		3

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127	Low-power asymmetric switching scheme with segmented capacitive architecture for SAR ADCs. Analog Integrated Circuits and Signal Processing, 2020, 102, 253-264.	0.9	3
128	Broadband crossed dipole circularly polarized antenna with parasitic ϵ -metal pillars. International Journal of RF and Microwave Computer-Aided Engineering, 2021, 31, e22786.	0.8	3
129	DTOF Image LiDAR With Stray Light Suppression and Equivalent Sampling Technology. IEEE Sensors Journal, 2022, 22, 2358-2369.	2.4	3
130	Time-Domain Power Distribution Network (PDN) Analysis for 3-D Integrated Circuits Based on WLP-FDTD. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2022, 12, 551-561.	1.4	3
131	Recent Advances and Trends in Voltage-Time Domain Hybrid ADCs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2575-2580.	2.2	3
132	3-D Compact Marchand Balun Design Based on Through-Silicon via Technology for Monolithic and 3-D Integration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1107-1118.	2.1	3
133	An 8-bit 208MS/s SAR ADC in 65nm CMOS. Analog Integrated Circuits and Signal Processing, 2013, 76, 129-137.	0.9	2
134	A Fast-Locking, Low-Jitter Pulsewidth Control Loop for High-Speed ADC. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2024, , 1-1.	2.1	2
135	CDS circuit with 0 to 18dB, 9-bit VGA functionality. Electronics Letters, 2014, 50, 158-159.	0.5	2
136	A low overhead load balancing router for network-on-chip. Journal of Semiconductors, 2016, 37, 115003.	2.0	2
137	A load balancing bufferless deflection router for network-on-chip. Journal of Semiconductors, 2016, 37, 075002.	2.0	2
138	Analysis and optimal distribution scheme for SAR-VCO ADCs. Microelectronics Journal, 2017, 70, 81-88.	1.1	2
139	A High-Resolution 2-GHz Fractional-N PLL With Crystal Oscillator PVT-Insensitive Feedback Control. IEEE Microwave and Wireless Components Letters, 2018, 28, 227-229.	2.0	2
140	PN-assisted digital background calibration of two-step ADC to over 14-bit accuracy. Analog Integrated Circuits and Signal Processing, 2018, 94, 75-82.	0.9	2
141	High-Efficiency Class-C ϵ -VCO With AFC-Based Phase Noise Compensation. IEEE Microwave and Wireless Components Letters, 2018, 28, 1125-1127.	2.0	2
142	Temperature-dependent characterizations on parasitic capacitance of tapered through silicon via (T-TSV). IEICE Electronics Express, 2018, 15, 20180878-20180878.	0.3	2
143	A High Gain, 808MHz GBW Four-Stage OTA in 65nm CMOS. Journal of Circuits, Systems and Computers, 2019, 28, 1950192.	1.0	2
144	Ultrawideband Power-Switchable Transmitter With 17.7-dBm Output Power for See-Through-Wall Radar. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1331-1335.	2.1	2

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145	A $\lambda/4$ -Band Integrated Tapered Array Antenna With Series Feed for Noncontact Vital Sign Detection. IEEE Transactions on Antennas and Propagation, 2021, 69, 3234-3243.	3.1	2
146	A TSV-Based 3-D Electromagnetic Bandgap Structure on an Interposer for Noise Suppression. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2022, 12, 147-154.	1.4	2
147	Optimization and Analysis of Microchannels Under Complex Power Distribution in 3-D ICs. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2022, 12, 537-543.	1.4	2
148	Gate Voltage Dependence Ultrahigh Sensitivity WS^2 , Avalanche Field-Effect Transistor. IEEE Transactions on Electron Devices, 2022, 69, 3225-3229.	1.6	2
149	Compact Interdigital Bandpass Filter, Diplexer, and Triplexer Based on Through Quartz Vias (TQVs). IEEE Transactions on Components, Packaging and Manufacturing Technology, 2022, 12, 988-997.	1.4	2
150	High-speed single-channel SAR ADC with a novel control logic in 65-nm CMOS. Analog Integrated Circuits and Signal Processing, 2017, 91, 503-511.	0.9	1
151	Electrical models of through silicon Vias and silicon-based devices for millimeter-wave application. International Journal of RF and Microwave Computer-Aided Engineering, 2018, 28, e21447.	0.8	1
152	Wideband Electromagnetic Distribution Characterization and Dielectric Analysis of Shielded-Pair Through-Silicon Via Using Recursive Approximation Algorithm. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 936-944.	1.4	1
153	A 32-GS/s Front-End Sampling Circuit Achieving >39 dB SNDR for Time-Interleaved ADCs in 65-nm CMOS. Journal of Circuits, Systems and Computers, 2021, 30, 2150143.	1.0	1
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